GC-NIP

Datasheet

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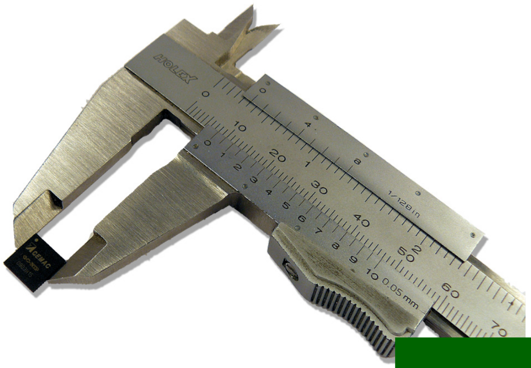

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Revision history

Date	Revision	Changes
21/05/2013	1.0	Initial version
17/06/2013	1.1	Operating mode changes
03/03/2014	1.2	Characteristic values updated Updated schematics
04/04/2017	1.3	change to new AMAC document layout

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1 Overview

The 2-channel interpolation circuit GC-NIP serves to increase the resolution of absolute position and angular measuring systems with 2 sinusoidal output signals (nonius signal). Aside from the calculation of the absolute position, the GC-NIP may also operate as one- or two-channel incremental measuring system.
The input signals are subjected to an AMAC-specific internal gain and offset control. Additionally, the phase deviation of the input signals can be adjusted statically by a digital potentiometer.
Dividing the signal period of the input signals up to 8,192 times, the incremental position on both channels is calculated as well as the absolute position using the nonius calculation. For the absolute position of a two-channel nonius system, a resolution of up to 22 bit can be achieved.

The distance information can be passed on to processing components via a fast SPI interface, an SSI interface, a BiSS interface or by conventional ABZ-square-wave signals.
Input and output of the GC-NIP are designed for 3.3V interfaces. The IC comprises six instrumentation amplifiers with adjustable gain factors. Encoders with voltage interface or measuring bridges can be connected directly. Sensors with current interface and photodiode-arrays are adapted by a simple external circuit. The IC operates on both single-ended or differential input signals. The noise of the sensor signals is prevented by a switching analog filter. Additionally, a digital hysteresis can suppress the edge noise of the output signals at low input frequencies and at standstill. Thus, is case of short-time disturbance of the input signals, a subsequent interpolation counter will operate without errors.
The quality of the signals issued by the sensors is monitored in the IC. For that purpose it is possible to activate 9 sources separately producing an error signal. For the calculation of the absolute position a set of sensor- or scale-specific correction coefficients can be placed in the EEPROM of the IC. In that way, harmonics of the sinusoidal signals or inaccuracies of the measuring scale do not lead to errors in the absolute position value. The determination of the correction coefficients is realized by a simple software-based calibration procedure.

Providing absolute position and incremental square-wave-signals (ABZ) in parallel, the GC-NIP is well-suited for the use in motor-feedback-systems. The four integrated output interfaces (ABZ/SPI/SSI/BiSS) and further features like the multistage trigger signal processing, the processing of distance coded reference marks, the possibility to adjust the reference mark as well as adjustment and storage of the zero position make the IC suitable for direct use in industrial controls or in fast absolute or multichannel incremental position measuring systems. A selectable master SPI interface allows the user to modify the SSI/BiSS-data by providing additional information, for example data from an external multiturn counter or error information.
The GC-NIP can be configured according to specific applications using the integrated EEPROM, via configuration inputs or via the serial interface (SPI/BiSS).

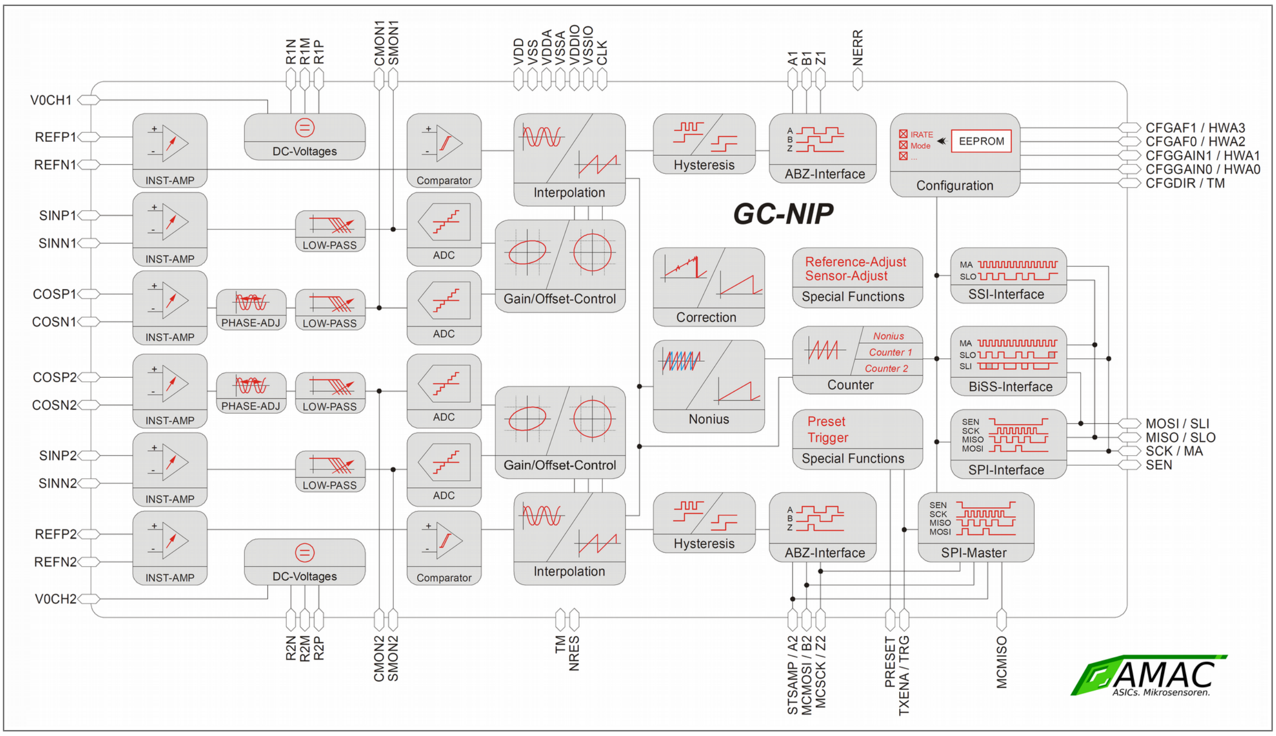


Figure 1: block diagram

2 Features

Interfaces	
Analog input	Sinusoidal / cosinusoidal / reference (index) signals, differential or single-ended Adjustable amplification for 660 mV_{PP} / 250 mV_{PP} / 120 mV_{PP} / 60 mV_{PP} Input frequency max.130 kHz for nonius calculation; max. 90 kHz for interpolation
ABZ	90° square-wave sequences (A/B/Z) Adjustable width of zero signal Z to ¼ or 1 period A/B Error signal; Interrupt signal for external processing Service signals for sensor adjustment
SPI	30-bit counter value for the interpolation channels Up to 22-bit resolution for the absolute position 9-bit sensor status information on each channel Compatible to Standard-SPI: 16-bit, MSB first, up to 15 MHz
SSI and BiSS	Up to 30-bit counter value 2-bit sensor status Gray code / binary code adjustable timing SSI ring operation
Additional inputs	Trigger input for storage of the measured value Preset signal for adjustment and storage of the counter values Reference position alignment using external signal
Configuration options	Integrated EEPROM Configuration inputs Serial Interface (SPI/BiSS)
Interpolation / nonius calculation / signal processing	
Interpolation rate	256 to 8192, divisible by 8 Adjustable Divider 1/2/4/8 for the AB-signals on each channel
Nonius pitch	Number of periods per turn for absolute position calculation Interpolation rate / [8 / 16 / 32 / 64]
Nonius correction	Correction coefficients stored in EEPROM Software based calibration process for determination of the correction coefficients
Signal correction	AMAC-specific digital controller for the offset, control range ±10% of the standard amplitude AMAC-specific digital controller for the amplitude, control range 60% … 120% of the standard amplitude Digital potentiometer with 64 steps for phase correction; selectable range ±5° or ±10° Input signal monitoring with configurable error indication
Suppression of disturbances	Adjustable low pass filter 10 kHz, 75 kHz, 150 kHz Digital hysteresis for suppression of the edge noise at the output (configurable 0...7) Selectable minimum edge distance at the output (bandwidth limitation)
Reference signal processing	Adjustable reference mark position in 32 steps 0 … 360° Optional: high precision alignment of the reference mark position (configuration via external signal possible) Processing of distance coded reference marks Measured-value trigger at the reference mark position
Miscellaneous	Optional Master-SPI interface for output and manipulation of SSI/BiSS-Data 2-stage measured value trigger Constant delay between sampling and measurement value for all resolutions
Important characteristics	
Package	QFN64 (9 x 9 mm)
Operating voltage	3.3V
Temperature range	-40 … 125 °C
Max interface clock	SPI 15 MHz, BiSS 10 MHz, SSI 5 MHz

3 Ordering Information

Product Type	Description	Article Number
GC-NIP	Interpolation Circuit GC-NIP, QFN64	PR-44800-00
GC-LS	4-channel / analog Level-Shifter 5V to 3.3V, QFN32	PR-44500-00
GP-NIP	Demoboard for Interpolation circuit GC-NIP	PR-44810-00
USB to SPI converter	USB adapter for the SPI interface	PR-44025-10

4 Typical applications

Table 1: Applications overview

Signal form (Sensor)	**Application of GC-NIP**
Sinusoidal, Voltage	Direct connection of GC-NIP to sensor.
Sinusoidal, Current	Additional resistors required
Reference- (Index-) Track	Direct connection of GC-NIP to sensor.
Square wave	IC is not suitable in principle.
Signal Form (Sensor)	**Application of GC-NIP**
1 V_{pp} nominal	Use GC-LS for signal conversion or external resistors.
660 mV_{pp} nominal	Direct connection of GC-NIP to sensor.
330 mV_{pp} nominal	Use GC-LS for signal conversion or external resistors.
250 mV_{pp} nominal	Direct connection of GC-NIP to sensor.
120 mV_{pp} nominal	Direct connection of GC-NIP to sensor.
80 mV_{pp} nominal	Use GC-LS for signal conversion or external resistors.
60 mV_{pp} nominal	Direct connection of GC-NIP to sensor.
2 V_{pp} nominal	External resistors required (see 11).
Differential signal, DC-Reference Voltage 0.82...1.8V	Direct connection of GC-NIP to sensor.
Single-Ended, DC-Reference Source in Sensor	Direct connection of GC-NIP to sensor.
Single-Ended, DC-Reference Source not in Sensor	Direct connection of GC-NIP to sensor.
Photodiodes 0.5 μA_{pp}	External resistors required. (see 11).
Photodiodes 11 μA_{pp}...16 μA_{pp}	External resistors required. (see 11).
Resistive bridges (magnetic sensors)	Direct connection of GC-NIP to sensor.
Unstable amplitude of sensor	GC-NIP contains automatic controller for amplitudes.
Offset not correctable at sensor	GC-NIP contains automatic controller for offset.
Phase not correctable at sensor	GC-NIP contains potentiometer for phase correction.
Variable Reference mark position	Reference mark position is freely adjustable.
Distance coded reference marks	Evaluation support via SPI using the internal trigger-function.

Subsequent processing	**Application of GC-NIP**
Interface to microcontroller/DSP/FPGA	Use SPI-Interface
Interface to external interpolation counter	AB-Interface for both channels
Usage on industrial control	SSI, BiSS or ABZ-Interface
System includes more than one channel	2 incremental interpolation channels included. Possibility to use simultaneously on only one SPI-Bus
Real-Time-System / equidistantly measurement	Constant propagation delay for all resolutions, trigger input
IC-Configuration	Integrated EEPROM, all registers are configurable via SPI/BiSS
Signal specification LVCMOS	In-/Outputs used directly
Signal specification RS422	Driver-IC required

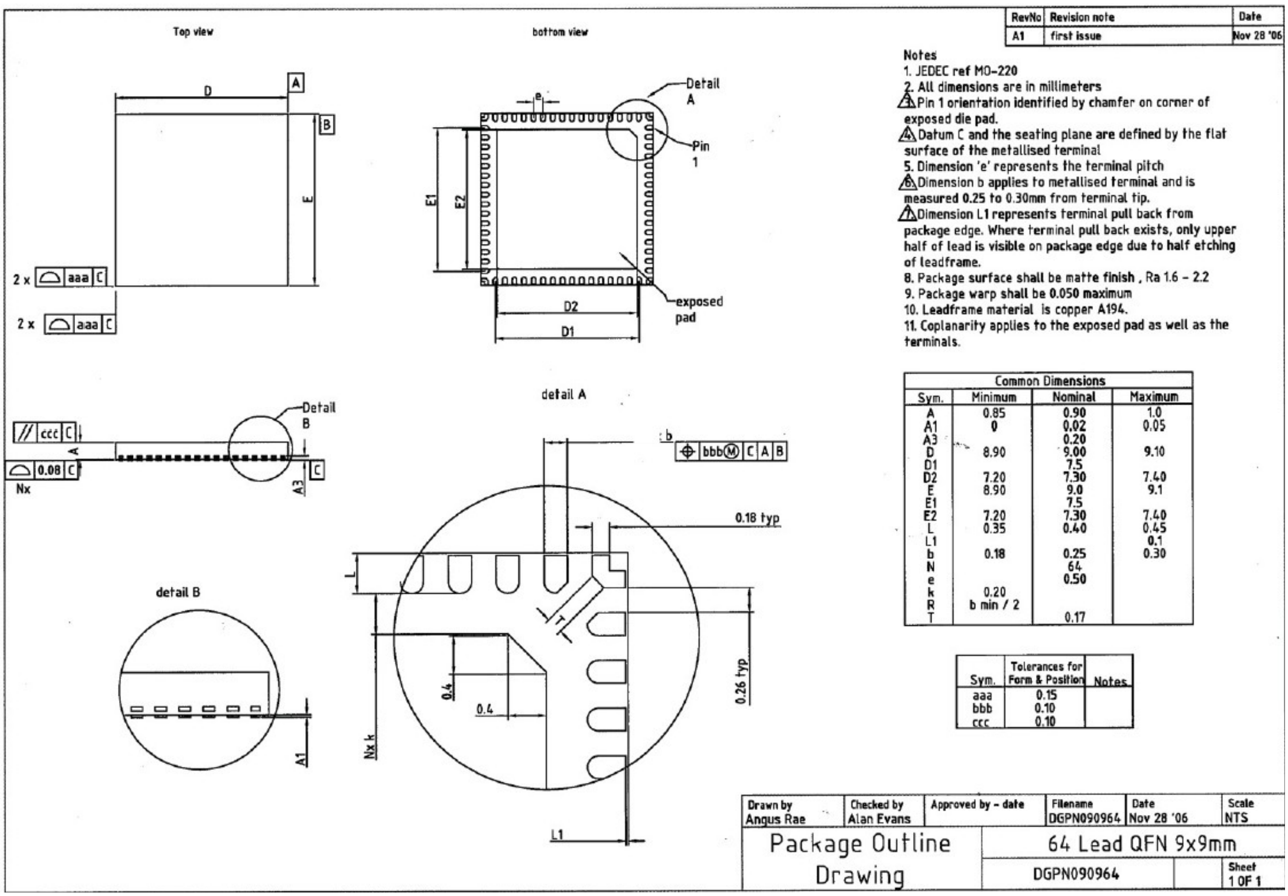
Maximum signal frequencies	
Rotary encoder: f_{max} = (revolutions / minute)·(signal periods / revolution) / 60	
Linear encoder: f_{max} = (v_{MAX} [in m/s] / (signal periods [in mm]) · 1000	
f_{max} < 150 kHz	All interpolation rates up to 8192 via SPI/SSI/BiSS
f_{max} < 23 MHz / Interpolation rate	If ABZ-outputs are used
Max frequency of interpolation counter on ABZ known	Configuration of the minimum edge distance possible via `CFGTPP`

5 Package

Table 2: Pin list QFN64

Pin	Name	Type	Description
1	VDDA	Power	Supply voltage analog +3.3V
2	VSSA	Power	Analog GND
3	R2P	Analog	ADC2-reference voltage high
4	R2M	Analog	ADC2-reference voltage mid
5	R2N	Analog	ADC2-reference voltage low
6	SMON2	Output analog (Buffer)	Monitor Output at instrumentation amplifier sine channel 2
7	CMON2	Output analog (Buffer)	Monitor Output at instrumentation amplifier cosine channel 2
8	N.C.	n.c.	Do not connect
9	VDD	Power	Supply voltage digital +3.3V
10	VSS	Power	Digital GND
11	CFGAF1/HWA3	Input digital / Pull-Down	Configuration analog filter / HWA<3>
12	CFGAF0/HWA2	Input digital / Pull-Down	Configuration analog filter / HWA<2>
13	SCK/MA	Input digital / Pull-Down	SPI/BiSS/SSI: clock
14	SEN	Input digital / Pull-Up	SPI: select / during Reset: select interface SPI / BiSS or SSI
15	MOSI/SLI	Input digital / Pull-Down	SPI/BiSS: data in GC-NIP
16	MISO/SLO	Output digital / Open-Drain	SPI/BiSS/SSI: data out GC-NIP
17	N.C.	n.c.	Do not connect
18	VDDIO	Power	Supply voltage digital (IO) +3.3V
19	VSSIO	Power	Digital GND
20	MCSCK / Z2	Output Digital / Tristate	Controller interface – clock / Output for Zero signal Z (reference signal)
21	MCMOSI / B2	Output Digital / Tristate	Controller interface – data out / Incremental output B channel 2
22	STSAMP / A2	Output Digital / Tristate	Controller interface – sync signal / Incremental output A channel 2
23	MCMISO	Input Digital	Controller interface – data in
24	TXENA / TRG	Input Digital	Controller interface – enable / trigger
25	CLK	Clock-Input	Clock
26	PRESET	Input digital / Pull-Up	Input for the preset function
27	CFGDIR / TM2	Input digital / Pull-Down	config. count direction nonius
28	Z1	Output Digital / Tristate	Output for Zero signal Z (reference signal) channel 1
29	B1	Output Digital / Tristate	Incremental Output B channel 1
30	A1	Output Digital / Tristate	Incremental Output A channel 1
31	VSSIO	Power	Digital GND
32	VDDIO	Power	Supply Voltage digital (IO) +3.3V
33	NERR	Output Digital / Open-Drain	Error signal
34	CFGGAIN0/HWA0	Input digital / Pull-Down	Configuration Gain / HWA<0>
35	CFGGAIN1/HWA1	Input digital / Pull-Down	Configuration Gain / HWA<1>
36	TM	Input digital	Test mode; Connect to VSS
37	NRES	In-/Output analog; Pull-Up	Reset
38	VS	Power	Test EEPROM
39	VCG	Power	Test EEPROM
40	VSS	Power	Digital GND
41	VDD	Power	Supply voltage digital +3.3V
42	CMON1	Output analog (Buffer)	Monitor Output at instrumentation amplifier cosine channel 1
43	SMON1	Output analog (Buffer)	Monitor Output at instrumentation amplifier sine channel 1
44	R1N	Analog	ADC1-reference voltage low
45	R1M	Analog	ADC1-reference voltage mid
46	R1P	Analog	ADC1-reference voltage high

47	VSSA	Power	Analog GND
48	VDDA	Power	Supply voltage analog +3.3V
49	N.C.	n.c.	Do not connect
50	REFP2	Input analog	Input Reference Signal positive channel 2
51	REFN2	Input analog	Input Reference Signal negative channel 2
52	REFP1	Input analog	Input Reference Signal positive channel 1
53	REFN1	Input analog	Input Reference Signal negative channel 1
54	V0CH1	Output analog (Buffer)	Mean voltage channel 1
55	SINP1	Input analog	Sinusoidal signal at input, positive channel 1
56	SINN1	Input analog	Sinusoidal signal at input, negative channel 1
57	COSN1	Input analog	Cosinusoidal signal at input, negative channel 1
58	COSP1	Input analog	Cosinusoidal signal at input, positive channel 1
59	COSP2	Input analog	Cosinusoidal signal at input, positive channel 2
60	COSN2	Input analog	Cosinusoidal signal at input, negative channel 2
61	SINN2	Input analog	Sinusoidal signal at input, negative channel 1
62	SINP2	Input analog	Sinusoidal signal at input, positive channel 1
63	V0CH2	Output analog (Buffer)	Mean voltage channel 2
64	N.C.	n.c.	Do not connect
EXP	VSS	Exposed Pad	Digital GND



RevNo	Revision note	Date
A1	first issue	Nov 28 '06

Notes
1. JEDEC ref MO-220
2. All dimensions are in millimeters
3. Pin 1 orientation identified by chamfer on corner of exposed die pad.
4. Datum C and the seating plane are defined by the flat surface of the metallised terminal
5. Dimension 'e' represents the terminal pitch
6. Dimension b applies to metallised terminal and is measured 0.25 to 0.30mm from terminal tip.
7. Dimension L1 represents terminal pull back from package edge. Where terminal pull back exists, only upper half of lead is visible on package edge due to half etching of leadframe.
8. Package surface shall be matte finish , Ra 1.6 – 2.2
9. Package warp shall be 0.050 maximum
10. Leadframe material is copper A194.
11. Coplanarity applies to the exposed pad as well as the terminals.

Common Dimensions			
Sym.	Minimum	Nominal	Maximum
A	0.85	0.90	1.0
A1	0	0.02	0.05
A3		0.20	
D	8.90	9.00	9.10
D1		7.5	
D2	7.20	7.30	7.40
E	8.90	9.0	9.1
E1		7.5	
E2	7.20	7.30	7.40
L	0.35	0.40	0.45
L1			0.1
b	0.18	0.25	0.30
N		64	
e		0.50	
k	0.20		
R	b min / 2		
T		0.17	

Sym.	Tolerances for Form & Position	Notes
aaa	0.15	
bbb	0.10	
ccc	0.10	

Drawn by	Checked by	Approved by – date	Filename	Date	Scale
Angus Rae	Alan Evans		DGPN090964	Nov 28 '06	NTS

Package Outline Drawing
64 Lead QFN 9x9mm
DGPN090964
Sheet 1 OF 1

Figure 1: Package QFN64

6 Start up Behaviour / Configuration Options

6.1 Reset

During reset of the IC, the digital interface is selected (SPI or SSI/BiSS) and all registers are initialized with their default values. The initialization of the circuit is performed either from the internal EEPROM or from configuration pins. The internal EEPROM has to be programmed with a valid identifier at EEPROM address 0x00 to be used for configuration after reset. The configuration of the interpolation rate is either done from the EEPROM (if valid) or with a fixed interpolation rate of 2000. Another valid identifier on EEPROM address 0x01 decides, if the correction coefficients – also located in the EEPROM of the IC – are loaded during reset and be used for absolute position calculation.

During the whole reset sequence, a pin - dependent on the selected interface - `NERR` or `MISO`, is maintained at L level. Up to this point, the serial interfaces may not be activated. Subsequently, the configuration registers can be modified using the SPI- or BiSS-interface. The following tables provide an overview of the configuration possibilities for the GC-NIP.

Table 3: Selection of the serial interface

Interface	Pin SEN reset value	BIT SSI 1)	Pin MISO / SLO	Pin MOSI / SLI	Pin SCK	Pin SEN	Ready-Signal
SPI	1	any value	SPI-MISO	SPI-MOSI	SPI-SCK	SPI-SEN	at MISO
SSI	0	1	SSI-DATA	-	SSI-MA	0	at NERR
BiSS	0	0	BiSS-SLO	BiSS-SLI	BiSS-MA	0	at NERR

1) Register CFGBiSS / Bit 31

Table 4: switching the configuration source

Content of EEPROM address 0x00	Configuration
unequal 0x134A	Basic configuration / see Tables 8 and 9 (Pin)
0x134A	read from EEPROM / Tables 8 and 9 (EEPROM)

Table 5: Configuration of the interpolation rate and nonius pitch

Content of EEPROM address 0x00	Bit IRMAP 1)	Configuration Source	Interpolation rate IRATE	Nonius pitch (Signal on channel 1)	Interpolation rate ABZ
unequal 0x134A	default value: 1	Manufacturer EEPROM	2000	125	2000
0x134A	0	EEPROM	any between [256 … 8192] divisible by 8	IRATE / [16,32,64, 128]	IRATE / [1,2,4,8]
0x134A	1	Manufacturer EEPROM	2000	125	2000 / [1,2,4,8]

1) Register CFG1 / Bit 3

Table 6: Configuration correction coefficients for nonius calculation

Content of EEPROM address 0x01	correction coefficients value
unequal 0x134A	All 0
0x134A	Read from EEPROM

6.2 Configuration

The IC can be matched to most varied measuring systems and subsequent electronic systems by way of the configuration registers. If the IC is initialized using the integrated EEPROM or a serial interface (SPI/BiSS), full configuration possibilities are available. If the initialization is performed via the configuration pins, selected parameters can be set externally. Table 7 below provides an overview of the configuration possibilities of the GC-NIP. Detailed description of the configuration register set can be found in sector 9 of this document.

Table 7: Configuration options

Parameter	Possible values	Register / Bit
Interpolation rate IRATE	Configurable interpolation table in EEPROM Alternative: fixed table in manufacturer-PROM Divider for square-wave-signals (ABZ) and counter Separate divider for channel 1 and 2	From EEPROM CFG1 / IRMAP CFG1 / IRDIV(1:0) CFG1 / IRD2SEL, CFG3 / IRDIV2(1:0)
Operating mode	Nonius + ABZ 2 Channel Calibration Mode	CFG1 / MODE(3:0)
Nonius pitch	Interpolation rate / [8 / 16 / 32 / 64]	From EEPROM
Nonius correction	Correction values Correction value resolution Activate / deactivate correction	From EEPROM CFG3 / MXSHR CFG3 / MXFEED
Min. edge interval t_{pp}	1, 2, 4, 8, 16, 32, 64, 128	CFG1 / CFGTPP(2:0)
Reference point	Enable, Disable, Delayed Width 1 Increment / 4 Increments Position 0°-360°, step size 11.25° Mode Reset, Trigger, adjust, distance coded Position 0°-360°, step size 360°/IRATE	CFG3 / DISZ(1:0), CFG3 /ZDEL(1:0) CFG2 / Z4 CFG2 / ZPOS CFG2 / ZMODE CFG3/NOSEL, NONOFFS
Nominal signal amplitude	660 mV_{pp}, 250 mV_{pp}, 120 mV_{pp}, 60 mV_{pp}	CFG1 / GAIN(1:0) alternative: Pins CFGGAIN(1:0)
Low pass filter (1dB)	150kHz, 75kHz, 10kHz (all +/-10%), Disable	CFG1 / CFGAF alternative: Pins CFGAF(1:0)
Digital hysteresis	0 (Disable), 1 … 7	CFG3 / DH(2:0)
Output signals A/B/Z	ABZ-Mode, DSP-Mode, sensor adjustment, Reference mark adjustment Optional Master-SPI on ABZ-channel 2	CFG1 / MODE(2:0) CFG1 / MODE(3)
Error processing	Masking, latch enable Output configuration in case of errors	CFG1 / Mxxx, Lxxx CFG1 / HLD, TRI
Phase correction	± 10° step width 0.15°, ±5° step width 0.08°	CFG2 / PH1(5:0) CFG2 / PH2(5:0) CFG2 / PHBER,
Gain controller	Default setting / time constant / Enable, Disable	CNTRLG, CFG3 / GAINCTL, DISCTL
Offset controller	Default setting / time constant / Enable, Disable	CNTRLO, CFG3 / OFFSCTL, DISCTL
Hardware address	0-15	CMD / SETHWA Pins HWA(3:0)
Special functions	Trigger pulse edge Preset function active / inactive Absolute position offset Counter preset position Absolute counter direction	CFG1 / TRGSLP CFG2 / PREENA NONOFFS, PREST2 PREST1,PREST2 Pin CFGDIR
Interface configuration	Format of the position values SPI-Mode synchronous, asynchronous BiSS interface active, inactive SSI-Timing BiSS-Timing BiSS data format 8Bit, 32 Bit SPI for manipulation of the SSI/BiSS-Data	CFGBISS / SSI20, GRAY, STBIT, STSEL CFG2 / ASYNC, SYNC(6:0) CFGBISS / SSI CFGBISS / SSITO, RING CFGBISS / BISSTO CFGBISS / READ32 CFG1 / MODE(3)
Power saving options	Deactivation of the Monitor-outputs Deactivation V0-Pins Deactivation of Channel 2 Deactivation of the nonius correction Deactivation of the reference mark processing	CFG2 / DISMON CFG2 / DISV0 CFG3 / DISCH2 CFG3 / MXFEED CFG3 / DISZ1, DISZ2

Table 8: Default configuration

Configuration	Default (EEPROM with factory settings)		Default (Pin)	
Analog	Phase correction	0°	Phase correction	0°
	Low pass -1dB	150 kHz	Low pass -1dB	configured via pin
	Nominal signal amplitude	660 mVpp	Nominal signal amplitude	configured via pin
	Power saving options	inactive	Power saving options	inactive
Interpolation Nonius	Interpolation rate	8000	Interpolation rate	2000
	Controller	active, timing 01	Controller	active, Timing 01
	Controller start values	Average	Controller start values	Average
	Reference mark position	at 45°	Reference mark position	at 45°
	Nonius pitch	125	Nonius pitch	125
	Correction	none	Correction	none
	Count direction	configured via pin DIR	Count direction	configured via pin DIR
	Power saving options	inactive	Powers saving options	inactive
ABZ output signals	Mode	ABZ	Mode	ABZ
	TPP	0	TPP	0
	Digital hysteresis	1	Digital hysteresis	1
	Z	active, 1 increment	Z	active, 1 increment
	Output in case of error	Hold	Output in case of error	Hold
	Power saving options	inactive	Power saving options	inactive
Error processing	Error monitoring	all errors	Error monitoring	all errors
	Error storage	inactive	Error storage	inactive
Special functions	Preset (Nonius)	inactive	Preset (Nonius)	always inactive
	Preset values	0x00	Preset values	0x00
	Nonius offset	0x00	Nonius offset	0x00
	Trigger pulse edge	falling	Trigger pulse edge	falling

Table 9: Default configuration interfaces

Configuration	Default (EEPROM with factory settings)		Default (Pin)	
SPI interface	Activate via Pin `SEN`		Activate via Pin `SEN`	
	Hardware-address at `HWA(3:0)`		Hardware-address at `HWA(3:0)`	
SSI interface	Activate via Pin `SEN`		Activate via Pin `SEN`	
	Timeout	20 µs @ 26 MHz, Ring mode	Timeout	20 µs @ 26 MHz, Ring mode
	Format	20Bit	Format	20Bit
	Direct output (no Simple-SPI)		Direct output (no Simple-SPI)	
BiSS interface	Hardware-address at `HWA(3:0)`		Hardware-address at `HWA(3:0)`	
	Timeout	19.7 µs @ 26MHz	Timeout	19.6 µs @ 26 MHz
	Format	30Bit Singleturn	Format	30Bit Singleturn
	Direct output (no Simple-SPI)		Direct output (no Simple-SPI)	

7 Functional description

7.1 Input amplifier / Low pass filter

The GC-NIP incorporates six instrumentation amplifiers with adjustable gain factors. Incremental encoders with voltage interface and measuring bridges can be connected directly. Sensors with current-interface are adapted by way of a simple external circuit (see 11.1). The IC operates with both, single-ended and differential input signals. The amplification is identical for all signals of the sensor (sinusoidal, cosinusoidal, index/reference). To adapt the GC-NIP to customized sensors, the mean voltage of the instrumentation amplifiers is provided at pins `V01` and `V02`.

The instrumentation amplifiers are connected to the internal AD converters. Alternatively, this connection is done directly or via a configurable low-pass filter. The cut-off frequencies given in Table 11 are achieved with an accuracy of +/-10%. The conversion range of the analog-digital-converter and the reference voltages of the instrumentation amplifiers are pre-adjusted, so that internal offset-error are already compensated. The signals on the input of the analog-digital-converters can be monitored using the pins `SMON1`, `CMON1`, `SMON2` and `CMON2`[1].

Table 10: Configuration signal amplitude (nominal) (Register `CFG1`)

CFG1/GAIN(1:0)	00	01	10	11
Input voltage for differential supply 1)(mV_{pp})	330	125	60	30
Input voltage $U_{DiffNom}$ nominal (mV_{pp})	660	250	120	60
Input voltage range for U_{Diff} (mV_{pp})	400...800	150...300	75...145	36...72
Input voltage for maximal ADC-range $U_{DiffMAX}$ (mV_{pp})	990	375	180	90
Reference voltage on `V0` nominal	1.1	1.1	1.1	1.1
Output voltage U_{MON} nominal on `SMON` / `CMON` (V_{pp})	1.27	1.27	1.27	1.27
Amplification (U_{MON} / U_{DIFF})	1.92	5.08	10.6	21.2

1) at each of the inputs `SINP`, `SINN`, `COSP`, `COSN`

Table 11: Configuration Low-pass-filter (Register `CFG1`)

Cut-Off-Frequency -1dB	CFG1/CFGAF(1:0)
150 kHz (-0.5dB)	00
75 kHz	01
10 kHz	10
low-pass disabled	11

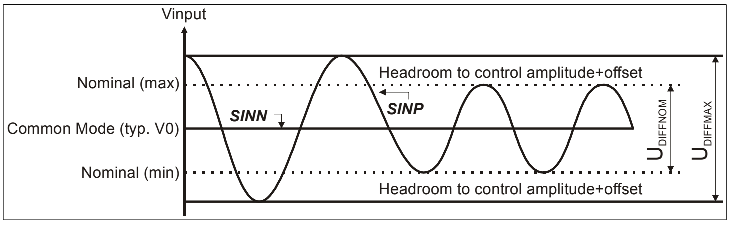


Figure 2: Input signals (single ended)

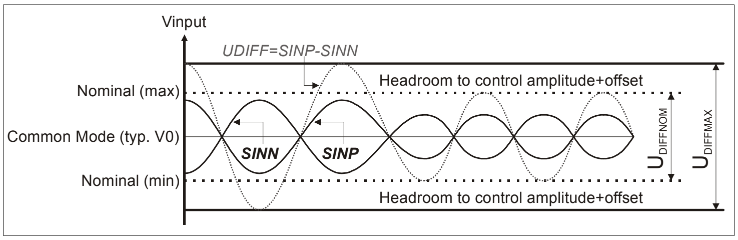


Figure 3: Input signals (differential)

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[1] The analog low-pass-filter must be activated when using the monitor-outputs (`CFG1/CFGAF` ≠ '11').

The input voltage for the instrumentation amplifiers is limited in a range from V_{in}=0.35V to VDDA-1.00V. According to the common-mode-voltage at the analog input, this may limit the operating range for the Gain-Configuration „00“ (V_{NOM} = 660 mV_{pp}).

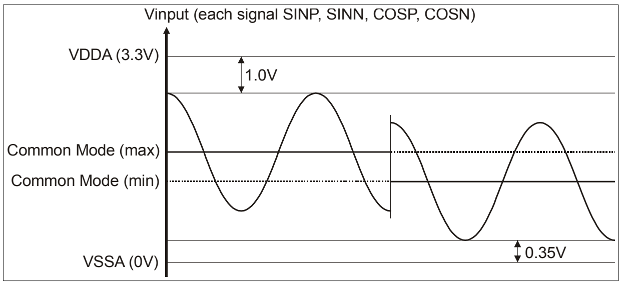


Figure 4: CMIR (input signals)

Exemplary, the following table shows combinations for common-mode-voltage and supply voltage for single-ended input signals with maximum amplitude of 880mV_{pp} and maximum offset of ±70 mV:

Table 12: Example: Common-mode input voltage (CMIR)

VDDA	Common-mode voltage (Min)	Common-mode voltage (Max)
3.30V	0.82V	1.83V
3.15V	0.82V	1.63V
3.00V	0.82V	1.53V

7.2 Signal correction

The input signals are subjected to an AMAC-specific internal gain and offset control. The amplitudes are controlled in the range between 60 % and 120 % of the standard amplitude. The control range for the offset of the two input signals is ± 10% of the nominal amplitude. The phase displacement of the input signals can be corrected statically in 64 steps using a digital potentiometer. The setting range of the phase is set to approx. +/-5° or approx. +/-10° by way of a configuration bit.

After resetting the IC, start values to correct amplitude and offset of the input signals are loaded from the EEPROM. If the EEPROM content is not marked valid (see 4), these values are set to the center of the control range. The full measuring accuracy of the IC, however, is only achieved after settling of the internal signal control after about 10...50 periods of the input signals. Alternatively, start values for the controller can be stored in EEPROM, so that the settling time of the controller after reset of the IC can be shortened.

To achieve the maximum possible accuracy in the amplitude and offset control, the phase potentiometer must be matched with the sensor connected to the GC-NIP. Amplitude and offset errors are treated as a unit in the GC-NIP. This means that for particular applications a larger permissible error may be permitted for the respectively other parameter under certain circumstances. The attenuation of the controlled system implemented in the GC-NIP can be adjusted (registers `CFG3/GAINCTL` and `CFG3/OFFSCTL`).

Table 13: Signal correction

Parameter	as a percentage referred to the nominal amplitude (PEAK-PEAK)	as a percentage referred to the ADC-maximum (PEAK-PEAK)	in mV referred to the standard signal (0.66 Vpp)	in V on the pin SMON and CMON (PEAK-PEAK)
Maximal value at the input ($Vmax_{pp}$)	150	100	990	1.90
Nominal value of the input signal ($Vnom_{pp}$)	100	66.7	660	1.27
Guaranteed control range for the amplitude	60... 120	40... 80	400... 800	0.76 … 1.52
Setting range of the amplitude controller	56... 168 1)	38... 112 1)	370... 1110 1)	0.71 … 2.13 1)
Vector monitoring2)	30	20	200	0.38
Guaranteed control range for the offset (sensor)	±15	±10	±70	±0.133
Setting range of the offset controller	±25	±17	±165	±0.315

1) The setting range for the amplitude is greater than the control range of the ADC.
2) An aggregate signal from sine and cosine is monitored. See chapter 7.5 Bit VLOW

7.3 Interpolation / nonius calculation

The signal periods of the analog sinusoidal and cosinusoidal signals are divided according to the selected interpolation rate and provided to the serial interfaces (SPI/SSI/BiSS) as phase and count value. In parallel, square-wave sequences with 90° phase shift (A/B/Z signals) are generated.

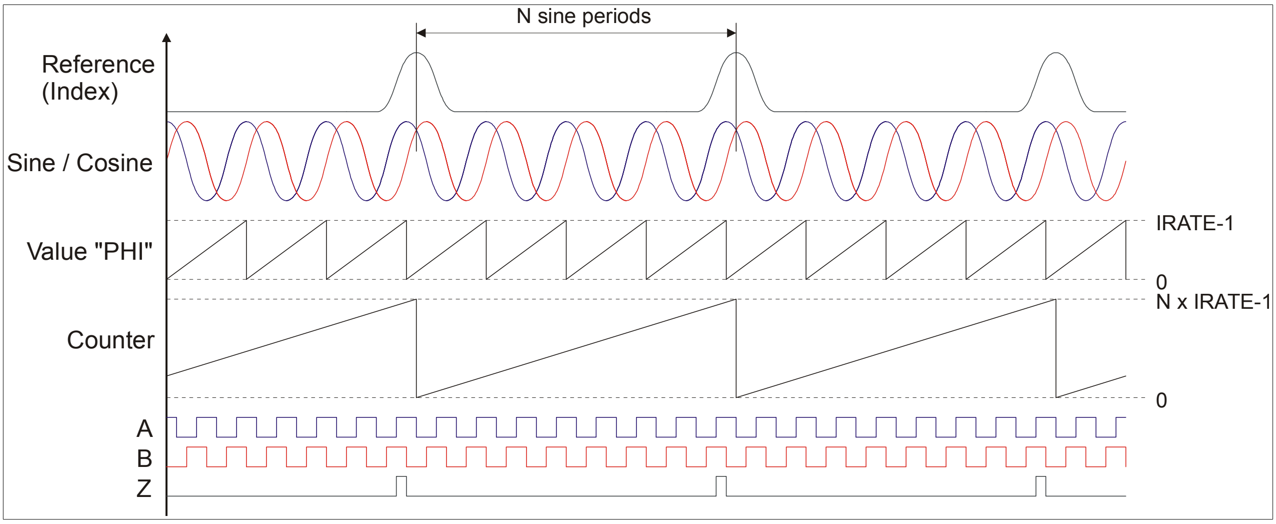


Figure 5: Interpolation

Using the phase values of the two channels and the vernier scale (nonius) method, the absolute position of the sensor is determined on the measuring scale. Errors of the sensor signal or resulting from inaccuracies of the measuring scale can be suppressed by way of an integrated correction. Therefore, 16 correction coefficients, determined by a software-based calibration algorithm, can be stored in the IC's internal EEPROM.

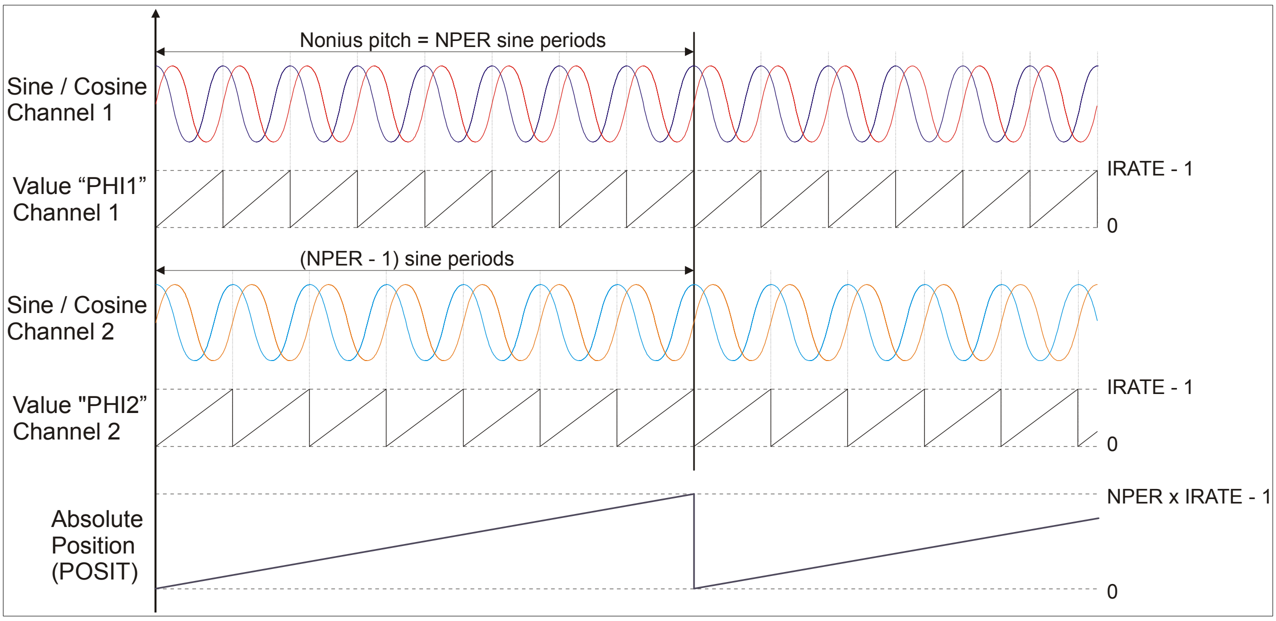


Figure 6: Nonius calculation

Table 14: Operating modes of the GC-NIP

Mode	CFG1/Mode'(3:0)	Sensor type	Measuring values
Nonius + ABZ	X000	Nonius sensor	Register CNT1: Incremental position channel 1 Register CNT2: Incremental position channel 2 Register POSIT: Absolute position [1] SSI/BiSS: Absolute position [1] ABZ1: Incremental signals channel 1 ABZ2: Incremental signals channel 2
Two channel	X000	2 independent sensors	Register CNT1: Incremental position channel 1 Register CNT2: Incremental position channel 2 Register POSIT: Incremental position 1 and/or 2 [1] SSI/BiSS: Incremental position 1 and/or 2 [1] ABZ1: Incremental signals channel 1 ABZ2: Incremental signals channel 2
Calibration	0101	Nonius sensor	Register CNT1: Incremental position channel 1 Register CNT2: Incremental position channel 2 Register POSIT: Absolute position [1] SSI/BiSS: Absolute position [1] ABZ1: Test signals for sensor adjustment ABZ2: Test signals for sensor adjustment

[1] The content of register `POSIT` is selected via `CFGBiSS/STSEL(1:0)` (see Register description)

7.3.1 Interpolation rate / nonius pitch

The term 'interpolation rate' (`IRATE`) is here understood as the number of increments, into which the sinusoidal/cosinusoidal period of the input signals is divided. 'Nonius pitch' describes the number of periods of the input signals, where the absolute position can be clearly assigned using the vernier (nonius) method. Possible interpolation rates for the nonius calculation of the GC-NIP can be selected between 256 and 8192 and must be divisible by 8. Additionally, the interpolation rate for the integrated interpolation counters and the square-wave-signal outputs (A/B) can be divided by a selectable factor (`IRDIV`) of 1, 2, 4 or 8 (both channels independently). The divided interpolation rate of the incremental counters corresponds the number of signal transitions at the A/B outputs per input signal period. The number of square-wave periods at the outputs `A` and `B` amounts to ¼ of the divided interpolation rate. The nonius pitch (`NPER`) is selectable from the values `IRATE/8`, `IRATE/16`, `IRATE/32` or `IRATE/64`.

Following table shows possible combinations and limitations of interpolation rate and nonius pitch for different interfaces and use cases.

Table 15: Selecting interpolation rate and nonius pitch

Interface / use case	Interpolation rate	Requirement/Limitation	Possible values for nonius pitch
Singleturn Nonius	IRATE from EEPROM 256 … 8192	IRATE is divisible by 8	NPER = IRATE / DIV DIV = [8, 16, 32, 64] If DIV = 8: IRATE ≤ 4096
Internal interpolation counter	IRATE from EEPROM / IRDIV IRDIV = [1, 2, 4, 8]	IRATE is divisible by 8	No influence
A/B-Output	IRATE from EEPROM / IRDIV IRDIV = [1, 2, 4, 8] IRDIV2 = [1, 2, 4, 8] (IRD2SEL = 1)	IRATE is divisible by 8 IRATE/IRDIV is divisible by 4	No influence

Example 1
The resolution of the absolute position should be at least 17 bit
The IC is used with measuring scales with a nonius pitch of 50 … 70 (channel 1)
The incremental resolution, using the AB-signals for a motor controller should be at least 10 bit

NPER	IRATE	DIV	Resolution	Bit	IRDIV	IRATE (ABZ)
50	3200	64	160000	17.29	2	1600
51	3264	64	166464	17.34	2	1632
52	3328	64	173056	17.40	2	1664
53	3392	64	179776	17.46	2	1696
54	3456	64	186624	17.51	2	1728
55	3520	64	193600	17.56	2	1760
56	3584	64	200704	17.61	2	1792
57	3648	64	207936	17.67	2	1824
58	3712	64	215296	17.72	2	1856
59	3776	64	222784	17.77	2	1888
60	3840	64	230400	17.81	2	1920

NPER	IRATE	DIV	Resolution	Bit	IRDIV	IRATE (ABZ)
61	3904	64	238144	17.86	2	1952
62	3968	64	246016	17.91	2	1984
63	4032	64	254016	17.95	2	2016
64	2048	32	131072	17.00	2	1024
65	2080	32	135200	17.04	2	1040
66	2112	32	139392	17.09	2	1056
67	2144	32	143648	17.13	2	1072
68	2176	32	147968	17.17	2	1088
69	2208	32	152352	17.22	2	1104
70	2240	32	156800	17.26	2	1120

Example 2
The maximum resolution for the absolute position should be achieved
The IC is used with measuring scales with a nonius pitch of 30 … 40 (channel 1)
The maximum interpolation rate for the AB-output is 128. This value has been calculated using the maximum input frequency and the maximum output frequency for the ABZ-outputs (see chapter 7.4).

NPER	IRATE	DIV	Resolution	Bit	IRDIV	IRATE (ABZ)
30	960	32	28800	14.81	8	120
31	992	32	30752	14.91	8	124
32	1024	32	32768	15.00	8	128
33	528	16	17424	14.09	8	66
34	544	16	18496	14.17	8	68
35	560	16	19600	14.26	8	70

NPER	IRATE	DIV	Resolution	Bit	IRDIV	IRATE (ABZ)
36	576	16	20736	14.34	8	72
37	592	16	21904	14.42	8	74
38	608	16	23104	14.49	8	76
39	624	16	24336	14.57	8	78
40	640	16	25600	14.64	8	80

7.3.2 Edge distance control / Interval time t_{pp} / Hysteresis

The minimum time interval t_{pp}, at which the output signals `A`,`B` and `Z` may switch, can be adjusted in binary steps between $1/f_{OSZ}$ and $128/f_{OSZ}$ using the configuration bits `CFG1/TPP(2:0)`. After switching one of the outputs, the subsequent edge of the other signal will only be visible at the IC output after the time t_{pp} has elapsed. Thus, in case of a short-time disturbance of the input signals, a subsequent interpolation counter will operate without errors. The configuration of the edge interval t_{pp} depends on the counter connected to `A`,`B` and `Z` (see section 11.6). Please note the discretization of time at the output of the IC due to the edge interval setting.

The GC-NIP uses a digital interpolation method. This causes the speed-proportional `A`/`B`/`Z` output signals to be overlaid by the inevitable quantization errors (the so called ±1INK errors) resulting from the A/D converters. The quantization noise can be suppressed by activating the digital hysteresis using register `CFG1/DH(2:0)`. This prevents switching of the outputs with static input signals. In this case, all output signals are delayed by one increment.

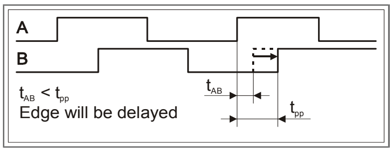


Figure 7: Edge interval setting

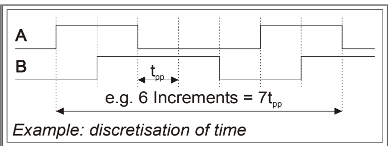


Figure 8: Discretization of time

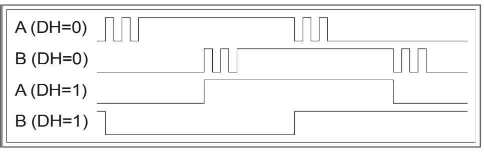


Figure 9: Digital hysteresis

7.3.3 Zero signal Z

The zero signal Z is generated when the sinusoidal and cosinusoidal analog signals display a phase angle defined by `ZPOS` (configured in register `CFG3/ZPOS(4:0)`) and at the same time the differential voltage of the reference inputs `REFP` and `REFN` exceeds the switching point. The default configuration for the phase angle is set to 45° at manufacturing (`ZPOS` = 4). The switching points of the reference signal must lie in the range between `ZPOS` ± [90°...150°]. The width of the zero signal `Z` (reference pulse) at the output can be switched between 1 and 4 increments, i.e. between ¼ and 1 period of the output signals `A` and `B`. If the IC is configured to the reference width of 1 increment (¼ period), the outputs `A` and `B` carry H level with activated `Z` signal. The adjustment of the phase angle for matching the IC to the reference signal of the sensor is supported by the IC. Setting `ZPOS` can be done using test signals or the trigger mode for reference point adjustment (see section 7.6.3 and 7.7).

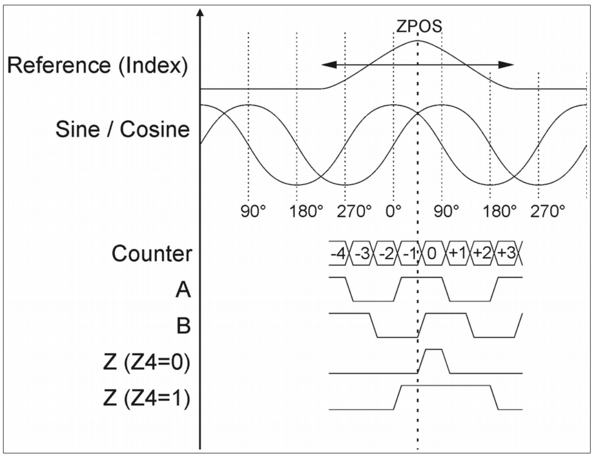


Figure 10: Interpolation (detail)

The relationship between the analog input signals, the output signals `A`, `B` and `Z` and the value of the incremental counter is shown in Fehler: Referenz nicht gefunden.

7.4 Maximum input frequency

The maximum input frequency depends on the selected interface at the output. If the square-wave-signals (`A`/`B`/`Z`) are used at the output, the maximum input frequency is limited by the interpolation rate for the AB-signals and the minimum edge interval (t_{pp}). When only using the internal count value (ABZ-output is deactivated in DSP-mode, see section 7.6) through the serial interface, the maximum input frequency is determined by the clock frequency of the circuit (f_{OSZ}). The maximum input frequency for the absolute position calculation (nonius) is limited by the error monitoring for the nonius result (`MNON`). The error reporting for exceeding the frequency limit is switched by the bit `MABZ` and `MFAST` in Register `CFG1`. Using the square wave signals at the output requires initializing both `MABZ` **and** `MFAST` with '1'. If the serial interface is used and the counters are read, `MABZ` can be deactivated. For only using the absolute position value via the serial interface, `MABZ` and `MFAST` can be deactivated.

Table 16: Maximum input frequency

Mode	MABZ	MFAST	MNON	Max. frequency for nonius calculation	Max. frequency for the counter	Max. frequency for the ABZ output
Nonius	0	0	1	$f_{MAX} \approx f_{OSZ}$ / 198	No error detection	No error detection
Counter	0	1	x		$f_{MAX} \approx f_{OSZ}$ / 280	No error detection
Square-wave,, $t_{pp} = N/f_{OSZ}$ $N = 2^{CFG1-TPP(2:0)}$ Interpolation rate ABZ $IRAB = IRATE / 2^{CFG1-IRDIV(1:0)}$	1	1	x		$f_{MAX} \approx 0.9 \cdot f_{OSZ} / (N \cdot IRAB) < f_{OSZ} / 280$	

ⓘ All values are valid with matched phase between the input signals (SIN and COS) and after the settling of the internal signal control. Up to this time, the input frequency may only amount up to 50% of the specified maximum frequency. Additionally, the maximum input frequency will be limited by the analog low-pass-filter at the input dependent on its configuration.

7.5 Sensor monitoring

The GC-NIP provides 9 sources on each channel for the signal monitoring. The sources can be activated or deactivated using the relevant bit in the register `CFG1`. Storage of the individual error flags can be activated using one further configuration bit each. The OR combination of the error signals saved or masked in this way is provided at the pin `NERR` (L-active). Additional warnings and error information and the individual error conditions can be read via the serial interface (SPI,SSI,BiSS). The behaviour of the square wave outputs in case of error can be configured. If the bit `HLD` in register `CFG1` is set to the value '1', the outputs will not change in case of error. Setting the bit `TRI` in register `CFG1` to '1' leads to setting the output to a high-impedance state in case of error.

ⓘ If the error signal has been activated or one of the error bits has been set in the result register, the current measurement result and all subsequent results must be discarded. After rectification of the error cause, the error bits can be reset by command `RESCNT` or by `PRESET` impulse. For measurements using a reference mark, it is imperative to pass through the reference point to be able to perform further absolute measurements.

Table 17: Overview sensor monitoring

NAME	Description	SPI	ABZ	SSI / BiSS
EVLOW	The signal vector generated from sine- and cosine-signal is too small.	Status bit	Error	Error
EADC	One or both A/D converters are overdriven.	Status bit	Error	Error
EOFFS	The offset controller has reached its limit.	Status bit	Error	Warning
EGAIN	The gain controller has reached its limit.	Status bit	Error	Warning
EFAST	The input frequency is too high.	Status bit	Error	Error
EABZ	The Signals `A`, `B` and `Z` are invalid.	Status bit	Error	-
ENON	The nonius calculation result is implausible.	Status bit	Error	Error

The error monitoring is configured by the user by switching the relevant bits in register `CFG1`. In principle, it is recommended to activate all monitoring sources by setting the bit to '1'. When not using the square wave outputs `A`, `B` and `Z`, the monitoring of the maximum ABZ-frequency (bit `MABZ`) can be switched off. If only the absolute position is used, the frequency monitoring can also be switched off via `MFAST`. See chapter 7.4for further information. If the GC-NIP is used as a one- or two-channel interpolation circuit without calculation of the absolute position (nonius), the monitoring of the nonius calculation can be switched off via `MNON`.

Table 18: Recommended configuration of the sensor monitoring

	ABZ-Interface	SPI-Interface	SSI-Interface	BiSS-Interface
Activated monitoring bits	EVLOW EADC EOFFS EGAIN EFAST (ENON) EABZ	EVLOW EADC EOFFS EGAIN (EFAST) (ENON)	EVLOW EADC EOFFS EGAIN (EFAST) (ENON)	EVLOW EADC EOFFS EGAIN (EFAST) (ENON)
Indication in case of error	Error signal on pin `NERR`	Error bit in register `STAT` Error bit in `POSIT` register Error signal at pin `NERR`	2 bits warning and error in the SSI data stream	2 bits warning and error in the BiSS data stream
Error storage	Deactivate	Activate	Activate	Activate
Clearing of the error storage	-	Command `RESCNT` PRESET-signal	`PRESET`-signal	Command `RESCNT` `PRESET`-signal
ABZ behaviour in case of error	Hold and/or Tristate	-	-	-
Register CFG1(31:16)	0x00FF 0x007F (no nonius calculation)	0x77F7 (nonius and counter) 0x73F3 (only nonius) 0x37B7 (only counter)	0x77F7 (nonius and counter) 0x73F3 (only nonius) 0x37B7 (only counter)	0x77F7 (nonius and counter) 0x73F3 (only nonius) 0x37B7 (only counter)

The following section describes the monitored sensor signal characteristics and shows the corresponding bits in the registers `CFG1` and `STAT`.

Vector error

The signal vector generated from the sinusoidal and cosinusoidal signals is smaller than 30 percent of the nominal amplitude. Usually, the cause is a partly or completely disconnected sensor. Another cause are input signals with very large offset at simultaneously low amplitude.

Masking	Error storage	STAT-Register	BiSS/SSI-SCD
Bit MVLOW	Bit LVLOW	Bit EVLOW	Bit1 – error

ADC error

One or both A/D converters are overdriven. The cause is that the signal amplitude is too high. Another cause are input signals with very large offset at simultaneously high amplitude. If appropriate pull-up or pull-down resistors are connected to the signal inputs, partly or fully disconnected sensors can also be detected by way of this error bit.

Masking	Error storage	STAT-Register	BiSS/SSI-SCD
Bit MADC	Bit LADC	Bit ESADC (sine) Bit ECADC (cosine)	Bit1 – error

Offset error

The offset controller has reached its limit. The cause is an excessive signal offset, a partly of fully disconnected sensor or an invalid value for initialization of the offset controller.

Masking	Error storage	STAT-Register	BiSS/SSI-SCD
Bit MOFF	Bit LOFF	Bit ESOFF (sine) Bit ECOFF (cosine)	Bit0 – warning

Amplification error

The gain controller has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly of fully disconnected.

Masking	Error storage	STAT-Register	BiSS/SSI-SCD
Bit MGAIN	Bit LGAIN	Bit ESGAIN (sine) Bit ECGAIN (cosine)	Bit0 – warning

Speed error

The input frequency is so high that no `A`/`B` signals can be generated or the direction can no longer be detected. The monitored frequency is different depending on whether an internal counter or the square wave outputs `A`/`B`/`Z` are used. See section 7.4. For sole use of the GC-NIP for absolute position calculation (nonius) the detection of this error can be deactivated (`MFAST` = 0).

Masking	Error storage	STAT-Register	BiSS/SSI-SCD
Bit MFAST	Bit LFAST	Bit EFAST	Bit1 – error

A/B/Z error

The signals `A`, `B` and `Z` are invalid. The cause is an excessive input frequency. The monitored frequency depends on the set minimum edge interval t_{pp}. This error bit will also be set, if the interpolation rate or the minimum edge interval t_{pp} is changed. The detection of this error must be deactivated, if the square wave outputs of the GC-NIP are not in use (`MABZ` = 0).

Masking	Error storage	STAT-Register	BiSS/SSI-SCD
Bit MABZ	Bit LABZ	Bit EABZ	-

Nonius error

The calculated absolute position is invalid. Cause are either errors of the input signals, which can not be internally corrected, or unfavourable combinations of the correction coefficients stored in the EEPROM. The nonius sensor shall be calibrated. See section 7.6.4.

Masking	Error storage	STAT-Register	BiSS/SSI-SCD
Bit MNON	Bit LNON	Bit ENON	Bit1 – error

7.6 Pins A/B/Z

The meaning of the signals at the pins `A`, `B` and `Z` can be modified using the bits `MODE(2:0)` in register `CFG1`. By default, the standard square wave sequences offset by 90° are generated. If only the internal counter of the IC is used, the mode „Controller/DSP“ can be activated. Thus, it is possible to carry out equidistant measurements, to synchronize additional components with the IC and to transfer measured values to a processing IC controlled by way of interrupts.

Additional modes are available providing test signals at the pins `A`, `B` and `Z` for sensor adjustment.

Setting the bit `CFG1/MODE(3)` to '1' enables a SPI-Master interface at the `ABZ`-pins of channel 2. If enabled, this SPI-Master cyclical sends the actual position value (register `POSIT`). Simultaneously, the data of the receiving register of the Master-SPI is used as value for the BiSS/SSI-stream data. This way, the position value can be read and modified from outside, i.e. to provide additional information from a battery powered multiturn-counter, or to transmit additional error information to a control. Also see section 8.4.

Table 19: ABZ modes

Mode	CFG1/MODE	A1	B1	Z1	A2	B2	Z2	TRG	Counter 1/ABZ1	BiSS/SSI
ABZ and nonius	00 00	A1	B1	Z1	A2	B2	Z2	TRG	from PHI1	direct
DSP and nonius	00 01	IRQ	StartSample	ZCNT1	IRQ	StartSample	ZCNT2	TRG	from PHI1	direct
Sensor adjust 1 1) Calibration	01 01	IR4C_1	IR4S_1	RCOMP_1	IR4C_2	IR4S_2	RCOMP_2	TRG Calibration trigger	from PHI1	direct
Sensor adjust 2 1)	01 10	IR8C_1	IR16C_1	NDEV1	IR8C_2	IR16C_2	NDEV2	TRG	from PHI1	direct
Sensor adjust Z	01 11	REFSync1	ZCNT1	Z1	REFSync2	ZCNT2	Z2	TRG	from PHI1	direct
ABZ and nonius	10 00	A1	B1	Z1	StartSample	MCMOSI	MCSCK	TXENA	from PHI1	Indirect via external controller
DSP and nonius	10 01	IRQ	StartSample	ZCNT1	StartSample	MCMOSI	MCSCK	TXENA	from PHI1	Indirect via external controller

1) For adjustment of the sensor signals the value `ZPOS` in register `CFG2` has to be configured to 00000

7.6.1 Standard ABZ (mode X000 and X010)

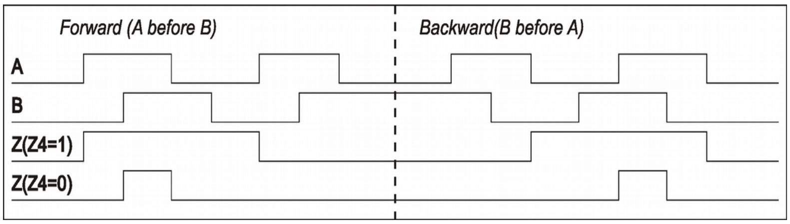


Figure 11: ABZ-Signals

7.6.2 Controller / DSP (mode X001 and X011)

If the measured values of the GC-NIP are transferred exclusively via the serial interface (SPI/BiSS/SSI), additional signals can be provided at the pins `A`, `B` and `Z`. The pin `NERR` maintains its meaning. It is designed as an open-drain pin, so that the error signals of several ICs can be connected to each other. The detection of ABZ-errors must be deactivated in mode Controller/DSP by writing '0' to `CFG1/MABZ`.

Table 20: DSP-Mode

Pin	Signal	Meaning
A	nINT	Interrupt; L-active; an active signal indicates that at least one of the trigger holding registers is occupied. A read access to the register `MVAL` provides the 'oldest' measured value saved in the registers. The interrupt can be triggered either by the reference signal at the input or by a signal at the pin `TRG` . See section 7.7.
B	StartSample	Synchronous signal; this signal delivers the sampling time of the integrated ADC. It can be used to synchronize further systems.
Z	ZCNT	Counter zero signal; this signal indicates that the internal counter of the GC-NIP is reset at the reference point (index point).

7.6.3 Reference point adjustment (sensor adjustment Z - mode 0111)

The phase value for detection of the reference mark (index point) can be moved within one sine period to match different sensors (see Figure 10). The adjustment can be configured in two step sizes; see Table 21.

Table 21: Reference point adjustment

Reference point position	Coarse adjustment	Fine adjustment
Configuration	`CFG3/NOSEL` = 0	`CFG3/NOSEL` = 1
Set position in register:	CFG2/ZPOS	NONOFFS
Step size	11,25°	360° / Interpolation rate
Comments	Adjustment value is used for both channels	Both channels can be configured separately. Offset value for the nonius calculation is **not** available.

For adjustment of the reference point position, test signals can be provided at the pins `A`, `B` and `Z` (see Figure 12). Additionally, the measured value trigger can be used for adjustment by setting the configuration bits `CFG2/ZMODE(1:0)` to „01“. This way, the GC-NIP triggers the counter on detection of the reference point. Reading the Register `MVAL` (with `CFGBiSS/STSEL` = 01 for channel 1 or `CFGBiSS/STSEL` = 10 for channel 2) provides the values `TRGVAL1` and `TRGVAL2` (see Figure 12, Table 22). In regard to the interpolation rate, the width of the reference signal and the position of the index signal related to the input signals can be calculated.

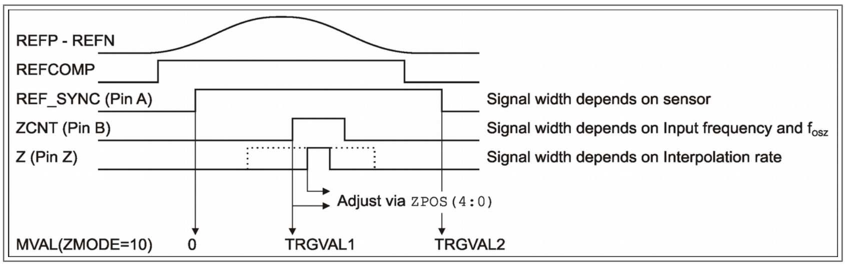


Figure 12: Adjustment of the reference (index) point

Table 22: Example: Reference point adjustment using the trigger mode

Value	Coarse adjustment (`CFG3/NOSEL` = 0)	Fine adjustment (`CFG3/NOSEL` = 1)
Width of the reference signal	Zwidth = TRGVAL2/IRATE·360°	Zwidth = TRGVAL2/IRATE·360°
Position of the reference signal	Zstart = Value ZPOS·11.25° - TRGVAL1/IRATE·360°	Zstart = (ZPOSCH12 – TRGVAL1)/IRATE·360°
Target position	TRGVAL1 = TRGVAL2/2	TRGVAL1 = TRGVAL2/2
New calculated position value	ZPOS_new = (Zstart + Zwidth/2)/11.25°	ZPOS_new = (Zstart + Zwidth/2)·IRATE/360°
Write to register	CFG2/ZPOS	NONOFFS

ⓘ The software for evaluation of the triggered values `TRGVAL1` and `TRGVAL2` should be able to handle the case, that no reference signal is available on the output (`Z`) or that the trigger values `TRGVAL1` or `TRGVAL2` are implausible because of multiple index signals. It is recommended to run reference point adjustment at a low signal frequency compared to the ICs clock frequency.

Another option for reference point adjustment is the usage of the preset function. If the preset is enabled via `CFG2/PREENA` = '1' and the fine adjustment is selected via `CFG3/NOSEL` = '1' an edge on the pin `PRESET` stores the actual phase values in Register `NONOFFS`. This way, the reference point position can be selected by an external impulse. For further information to the preset function see section 7.10.

7.6.4 Calibration mode (mode 0101)

The calibration mode of the GC-NIP serves to determine the correction coefficients which are used to enable the 2 track nonius calculation even with distorted sine- and cosine-input-signals. In calibration mode, the registers of the corrected input values (`CADC`) and a quadrant counter are held on an external event (command `TRGCAL` or pin `TRG`) and can be read via the SPI interface. Based on software, these values can be read for the whole period of the nonius scale and the 16 correction coefficients can be calculated and stored in the integrated EEPROM. The evaluation of the coefficients can be realized with the software GC-NIP-Monitor.

7.6.5 Sensor adjustment (mode 0101 and 0110)

The IC GC-NIP performs an automatic adjustment of amplitude and offset of both signals, sine and cosine, of the encoder. It is reasonable to correct static errors of the sensor previously to use the full control range for dynamic errors. Therefore, subsidiary signals at the pins `A`,`B`, and `Z` are available in the modes „sensor adjustment 1“ and „sensor adjustment 2“. The output signals of the instrumentation amplifiers can be measured at the pins `SMON` and `CMON`1). A description of the adjustment sequence can be found in Table 23. Additionally, the following figures show typical signal characteristics.

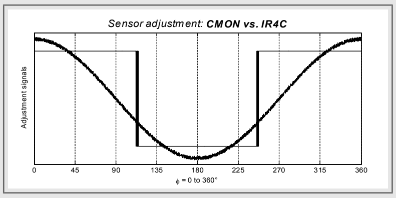
1) The analog low-pass-filter must be activated when using the monitor-outputs (`CFG1/CFGAF` ≠ '11').

Table 23: Sensor adjustment

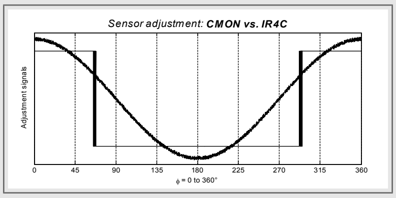
No.	Adjustment	Settings of the registers `CFG1` / `CFG2`	Instruction
1	Amplitude Sine/Cosine	Setting of the gain factor	Move sensor; measure on the pins `SMON` and `CMON`. Adjustment until both amplitudes display approx. 1.27V_{pp}.
2	Reference	Mode: „sensor adjustment 1“	Measure signal `REFCOMP`; adjustment until the signal width corresponds to approx. one period of the sinusoidal signals.
3	Offset Cosine	Mode: „sensor adjustment 1“ Deactivate controller (Bit `DISCTRL` = 1). Controller disabled; correction values in the middle of the setting range	Move sensor; measure on `CMON` and signal `IR4C`. Adjustment until mark-to-space ratio at `IR4C` is 50% of the period at `CMON`.
4	Offset Sine	Mode: „sensor adjustment 1“ Deactivate controller (Bit `DISCTRL` = 1). Controller disabled; correction values in the middle of the setting range	Move sensor; measure on `SMON` and signal `IR4S`. Adjustment until mark-to-space ratio at `IR4S` is 50% of the period at `SMON`.
5	Phase (coarse)	Mode: „sensor adjustment 2“ Activate controller (Bit `DISCTRL` = 0).	Move sensor; measure on the pins `CMON` and signal `IR16C`, coarse adjustment of the phase until all edges on `IR16C` are distributed evenly within the sinusoidal period.
5	Phase (fine)	Mode: „sensor adjustment 2“ Activate controller (Bit `DISCTRL` = 0).	Move sensor; measure at `CMON` and signal `NDEV`, adjust phase until frequency at `NDEV` does not correlate with the frequency of the sinusoidal signal.
6	Amplitude equality	Mode: „sensor adjustment 2“ Deactivate controller (Bit `DISCTRL` = 1). Controller disabled; correction values in the middle of the setting range	Move sensor, measure at `CMON` and signal `IR8C`, adjust signal amplitudes until all edges at `IR8C` are distributed evenly within the sinusoidal period.

Adjustment offset cosine – signals `CMON` and `IR4C` (pin `A`)
Mode '0101' (sensor adjustment 1), signal controller inactive / correction values in the middle of the setting range

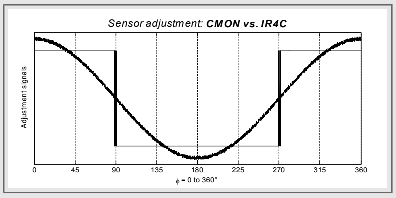
Offset cosine **positive**
Duty cycle `IR4C` > 50%



Offset Cosine **negative**
Duty cycle `IR4C` < 50%

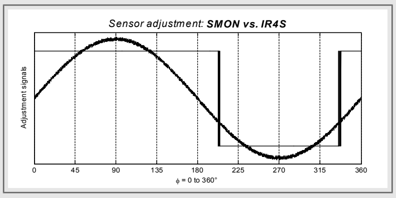


Offset cosine **adjusted**
Duty cycle `IR4C` = 50%

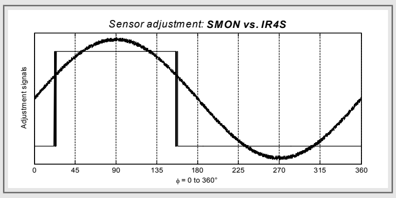


Adjustment offset sine – signals `SMON` and `IR4S` (pin `B`)
Mode '0101' (sensor adjustment 1), signal controller inactive / correction values in the middle of the setting range

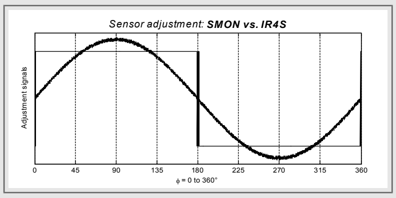
Offset sine **positive**
Duty cycle `IR4S` > 50%



Offset sine **negative**
Duty cycle `IR4S` < 50%

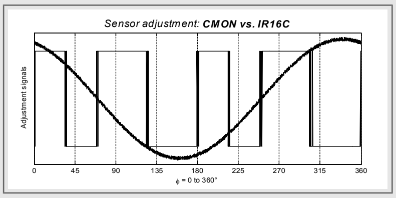


Offset sine **adjusted**
Duty cycle `IR4S` = 50%

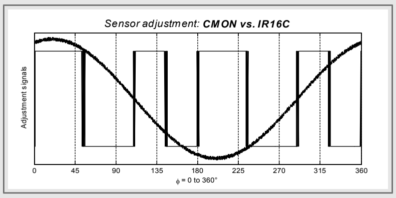


Adjustment phase (coarse) – signals `CMON` and `IR16C` (pin `B`)
Mode '0110' (sensor adjustment 2), signal controller active

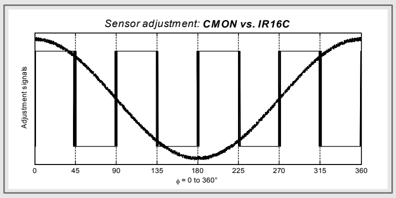
Phase between cosine and sine **> 90°**
Duty cycle `IR16C ≠` 50%
H-L-edge `IR16C` at φ < 45°



Phase between cosine and sine **< 90°**
Duty cycle `IR16C ≠` 50%
H-L-edge `IR16C at` φ > 45°

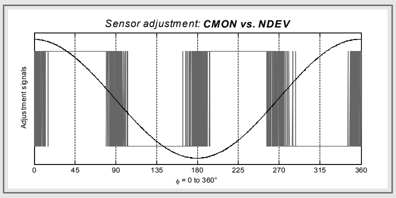


Phase between cosine and sine **adjusted**
Duty cycle `IR16C =` 50%
H-L-edge `IR16C` at φ = 45°

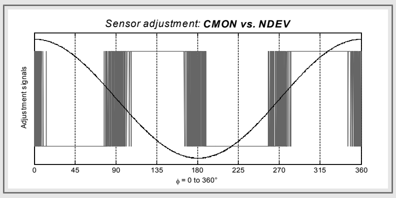


Adjustment phase (fine) – signals `CMON` and `NDEV` (pin `Z`)
Mode '0110' (sensor adjustment 2), signal controller active

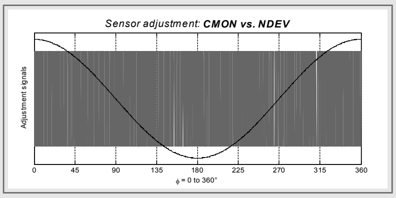
Phase between cosine and sine **>≈ 90°**
Frequency(`NDEV`) ≈
½·Frequency(`CMON`)
H-level `NDEV at` φ = 45°



Phase between cosine and sine **<≈ 90°**
Frequency(`NDEV`) ≈
½·Frequency(`CMON`)
L-level `NDEV` at φ = 45°

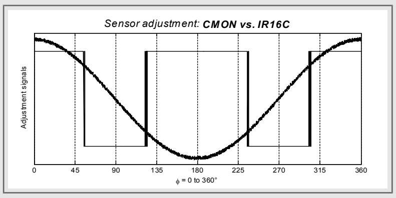


Phase between cosine and sine **adjusted**
Frequency(`NDEV`) >> Frequency(`CMON`)

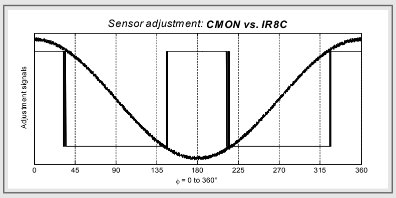


Adjustment amplitude coincidence – signals `CMON` and `IRC8` (pin `A`)
Mode '0110' (sensor adjustment 2), signal controller inactive / correction values in the middle of the setting range

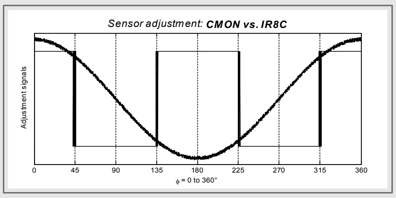
Ampl. cosine **greater than** Ampl. sine
Duty cycle `IR8C` > 50%



Ampl. cosine **lower than** Ampl. sine
Duty cycle `IR8C` < 50%



Ampl. cosine and Ampl. sine are **equal**
Duty cycle `IR8C =` 50%



7.7 Measured value trigger

The GC-NIP contains two trigger holding registers. The current value of the `POSIT`-register can be written to one of these registers controlled by the hardware, for instance by signal edge at pin `TRG`. The respectively 'oldest' value from the trigger holding registers is provided when accessing the register `MVAL` for reading. If no value is saved, the current value of register `POSIT` is displayed. The trigger holding register is re-enabled after reading. The trigger source of the **next** value to be read from `MVAL` is saved in the status register `STAT` (bits `TRG` and `TRGZ`). Furthermore, the bit `TRGOVL` indicates whether a trigger pulse was lost, because both trigger holding registers were occupied when a new trigger pulse appeared. In Register `MVAL`, it can be detected from the bit `TRG`, whether the value was triggered by hardware event. If the IC is configured in mode („Controller/DSP“; see section 7.6.2), the signal `nINT` on pin `A` is switched to L-level, if one of the trigger holding registers is occupied. An example of the program sequence for reading the triggered values using the registers `MVAL` and `STAT` is shown in section 11.3.

Table 24: Trigger mode / reference mode

Trigger source	Usage
`TRG`-pin	Trigger event from an external device (i.e. measuring probe). Trigger by microcontroller for equidistant measurements.
Reference signal CFG2/ZMODE=„01“	Trigger by the reference (index) signal for evaluation in software.
Reference signal CFG2/ZMODE=„10“	Trigger by the reference (index) signal for adjustment of the reference position in software.
Reference signal CFG2/ZMODE=„11“	Trigger by the reference (index) signal for the evaluation of distance coded reference marks.

TRG-pin
The current count value is written to one of the two trigger holding registers by way of a signal edge at pin `TRG` The trigger edge (falling or rising) can be set using the bit `TRGSLP` in register `CFG1`.

Reference index trigger
Any occurrence of a reference index at the input triggers the actual position value (register `POSIT`) to be stored in one of the two trigger holding registers.

Adjustment of the reference index position
The method of adjusting the reference point position is described in section 7.6.3. A rising edge at the reference signal resets the internal counter. The detection of the index in the IC (at the configured phase angle) triggers the counter to be stored into the first trigger holding register. The falling edge at the reference signal at the input triggers the counter to be stored in the second trigger holding register. After the two trigger events, the bit `ZSTAT` in register `STAT` is set and the trigger processing is locked until release by one of the SPI/BiSS commands `RESCNT` or `CLRZ`. See Figure 12.

Processing of distance coded reference marks
The first reference mark resets the internal counter. The second reference mark triggers the counter to be stored in the first trigger holding register. After these two events, the bit `ZSTAT` in register `STAT` is set and the trigger processing is locked until release by one of the SPI/BiSS commands `RESCNT` or `CLRZ`. The distance between the two reference marks must be at lease two periods of the input signals. The calculation of the absolute position of the sensor from any further values is handled by the evaluation software. See section 11.5 and Figure 49 for more information.

7.8 Measured value register POSIT, CNT, MVAL and STAT

The interpolated counter values, the trigger holding values, the position values as well as the sensor monitoring information can be read out from various registers via the serial interfaces. Following table shows the measured value registers for the different interfaces. For the BiSS interface it can be chosen between register data (slow communication) and single-cycle-data (SCD; fast communication). Programming examples for reading the measured value registers are shown in section 11.3.

Table 25: Measured value registers

	SPI	SSI	BiSS
Register CNT1 / CNT2	Interpolation counter 30 bit Index status 1 bit Error status 1 bit	-	Interpolation counter 30 bit Index status 1 bit Error status 1 bit
Register POSIT	See Table 27 Error status 2 Bit	-	Use SCD
Register MVAL	Register MVAL: see Table 28 Error status 1 bit Trigger status 1 bit	-	-
Register STAT	Error status 19 bit Trigger status 3 bit Index status 2 bit	-	Error status 19 bit Trigger status 3 bit Index status 2 bit
SCD (BiSS) / SSI-data 1)	-	See Table 26 Error status 2 bit	See Table 26 Error status 2 bit 2 MSB: 00

1) This data can be modified by an externally connected microcontroller → see section 8.4

Content and format of the position data register (`POSIT`) can be selected in register `CFGBISS` using the bits `STBIT`, `STSEL` and `GRAY`. The configuration bits `STBIT(4:0)` describe the bit-length (LSB) of the position value. Unused MSB are set to '0'. The coding of the position data can be switched between gray-code (`GRAY` = 1) and binary-code (`GRAY` = 0). The value `STSEL` defines the content in the position data register `POSIT` (see table 26 and table 27).

Table 26: Position data SSI/BiSS/SPI

STSEL	Position data SSI1)	Position data BiSS	Position data SPI
00	30 Bit Position / 8-30 Bit Resolution 1 Bit Error / 1 Bit Warning	32 Bit Position / 8-30 Bit Resolution 1 Bit Error / 1 Bit Warning	30 Bit Position / 8-30 Bit Resolution 1 Bit Error / 1 Bit Warning
01	30 Bit Counter Channel 1 / 8-30 Bit Resolution 1 Bit Error / 1 Bit Warning	32 Bit Counter Channel 1 / 8-30 Bit Resolution 1 Bit Error / 1 Bit Warning	30 Bit Counter Channel 1 / 8-30 Bit Resolution 1 Bit Error / 1 Bit Warning
10	30 Bit Counter Channel 2 / 8-30 Bit Resolution 1 Bit Error / 1 Bit Warning	32 Bit Counter Channel 2 / 8-30 Bit Resolution 1 Bit Error / 1 Bit Warning	30 Bit Counter Channel 2 / 8-30 Bit Resolution 1 Bit Error / 1 Bit Warning
11	15 Bit Counter Channel 1 15 Bit Counter Channel 2 1 Bit Error / 1 Bit Warning	2 Bit unused 15 Bit Counter Channel 1 15 Bit Counter Channel 2 1 Bit Error / 1 Bit Warning	15 Bit Counter Channel 1 15 Bit Counter Channel 2 1 Bit Error / 1 Bit Warning

1) The length of the SSI-data depends on the configuration of bit `CFGBISS/SSI20` (32 or 20 bit)

Table 27: Configuration of the position data register POSIT(31:0)

STSEL	Register POSIT			
00	Nonius position (max. 30Bit)		ERROR (1Bit)	WARNING(1Bit)
01	Interpolation counter 1 (max. 30Bit)		ERROR (1Bit)	WARNING(1Bit)
10	Interpolation counter 2 (max. 30Bit)		ERROR (1Bit)	WARNING(1Bit)
11	Interpolation counter 2 (15Bit)1)	Interpolation counter 1 (15Bit)1)	ERROR (1Bit)	WARNING(1Bit)

1) It is recommended to use binary representation only (`GRAY` = 0) for `STSEL` = '11'

Table 28: Configuration of the position data register MVAL(31:0)

STSEL	Register MVAL			
00	Nonius position (max. 30Bit)		Trigger status (1 Bit)	ERROR(1Bit)
01	Interpolation counter 1 (max. 30Bit)		Trigger status (1 Bit)	ERROR(1Bit)
10	Interpolation counter 2 (max. 30Bit)		Trigger status (1 Bit)	ERROR(1Bit)
11	Interpolation counter 2 (15Bit)	Interpolation counter 1 (15Bit)	Trigger status (1 Bit)	ERROR(1Bit)

The register `MVAL` contains a triggered position value if bit 1 (Trigger status) is set. Otherwise, the actual value from the `POSIT` register is displayed. → see section 7.7

7.9 Count direction switch (pin DIR)

The configuration pin CFGDIR serves to set the count direction for the absolute (nonius) position calculation. The pin has no effect on the count direction of the two interpolation counters or the A/B output signals.

7.10 Counter preset / Nonius offset / Commands / Control signals

The reset values for the integrated interpolation counters, the nonius offset value and the reference point position can be configured. The GC-NIP contains the preset registers PREST1 and PREST2 and the nonius offset register NONOFFS, which allow the user to set the zero position of the sensor independent from a reference signal. In conjunction with the integrated EEPROM, the zero position can be stored during system power-down. An overview about available signals and commands is shown in table 29.

Table 29: Commands

Command / Signal	Action
Reference signal (at pin REFP/REFN)	Resets the counter to zero
Reset SPI/BiSS-command RESIC 1)	The registers PREST1 and PREST2, the controller parameters and the register NONOFFS are loaded from the EEPROM. The content of the preset registers (PREST1/PREST2) is transferred into the counter registers.
Reset SPI/BiSS-command RESIC 2)	The registers PREST1 and PREST2 and the register NONOFFS are not changed. The content of the preset registers (PREST1/PREST2) is transferred into the counter registers.
SPI/BiSS- Command RESCNT	The content of the preset registers PREST1 and PREST2 is transferred into the counter registers.
SPI/BiSS- Command RESCTL	The controller parameters are set to the center of their value range.
SPI/BiSS- Command WCFG	The registers PREST1, PREST2 and the controller parameters are written to the EEPROM.
SPI/BiSS- Command PRESET	If the bit CFG2/PREENA is set, the offset for the nonius position NONOFFS is re-calculated using the preset value for the nonius from register PREST2 and the new offset value (NONOFFS) is stored in the EEPROM.
Falling edge at pin PRESET	CFG3/NOSEL = 0 The content of the preset registers PREST1 and PREST2 is transferred into the counter registers. If the bit CFG2/PREENA is set, the offset for the nonius position NONOFFS is re-calculated using the preset value for the nonius from register PREST2 and the new offset value (NONOFFS) is stored in the EEPROM. CFG3/NOSEL = 1 If the bit CFG2/PREENA is set, the actual phase angle of both channels is written to the register NONOFFS and stored in EEPROM. The contents of register NONOFFS define the reference index position (fine adjustment of signal Z) (see register description and section 7.6.3)

1) if EEPROM is valid, see section 6.1 2) if EEPROM is invalid, see section 6.1

The signal on pin PRESET is debounced in the IC. After a falling edge of the signal, the signal event generation is locked for a time of $t_{debounce}$, which is about 60 ms for a clock frequency of 26 MHz. The function of the pin PRESET depends on the configuration bit CFG2/PREENA. Additionally, the configuration of CFG3/NOSEL switches the meaning of the register NONOFFS.

7.10.1 Nonius-Offset

Configuring the bit CFG3/NOSEL with '0' defines the register NONOFFS to be used as offset register for the nonius calculation. The content of the POSIT register is then calculated from the physical nonius position and the nonius offset (see 31). Using the preset function, the offset can be calculated in hardware, where the register PREST2 holds the target position for the absolute position (see 30 and 31).

Table 30: PRESET-Pin

CFG2/PREENA = 0	CFG2/PREENA = 1
The interpolation counter register CNT1 is loaded with the content of the PREST1 register.	The interpolation counter register CNT1 is loaded with the content of the PREST1 register.
The interpolation counter register CNT2 is loaded with the content of the PREST2 register.	The interpolation counter register CNT2 is loaded with the content of the PREST2 register.
	The offset for the nonius position is re-calculated using the actual position and the content of the PREST2 register.
	The calculated value for the nonius offset (NONOFFS) is stored in the EEPROM.

The following relationship applies for the registers PREST2, POSIT (Nonius = absolute position value) and NONOFFS:

Table 31: Nonius offset

Measurement	Preset-Function
POSIT = Nonius(PHI1,PHI2,CFGDIR) + NONOFFS	NONOFFS (new) = PREST2 - Nonius(PHI1,PHI2,CFGDIR) POSIT = Nonius(PHI1,PHI2,CFGDIR) + NONOFFS (new) = PREST2

7.10.2 Configuration of the reference point position

Setting the configuration bit `CFG3/NOSEL` to '1' defines the register `NONOFFS` to store the reference mark position for both channels. A signal edge at pin `PRESET` then stores the actual phase angle information (PHI1 and PHI2) to be used as reference point position. This way, the zero position of the internal counters and A/B signals can be set freely within one sine period (see Figure 13 and Table 32). The resolution of the phase angle information depends on the selected interpolation rate.

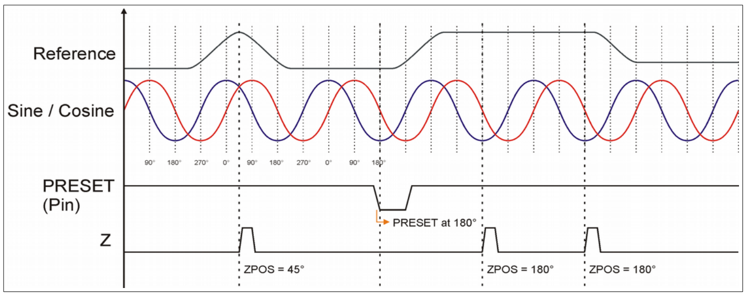


Figure 13: Fine adjustment of the reference point position

Table 32: `PRESET`-Pin `CFG3/NOSEL` = 1

`CFG2/PREENA` = 0	**`CFG2/PREENA` = 1**
The interpolation counter register `CNT1` is loaded with the content of the `PREST1` register.	The interpolation counter register `CNT1` is loaded with the content of the `PREST1` register.
The interpolation counter register `CNT2` is loaded with the content of the `PREST2` register.	The interpolation counter register `CNT2` is loaded with the content of the `PREST2` register.
The reference point position is loaded from register NONOFFS.	The actual phase angle of channel 1 is stored in register `NONOFFS`(15:0).
	The actual phase angle of channel 2 is stored in register `NONOFFS`(31:16).
	The register `NONOFFS` is stored in EEPROM.
	The reference point position is loaded from register NONOFFS.

Note: Since counter, controller and EEPROM are influenced by several sources, the following notes apply:

- During EEPROM access, the PRESET-signal is suppressed
- During EEPROM access, the command RESCNT is suppressed.
- During EEPROM access, the command WCFG is suppressed.
- If the PRESET signal is active during write access to the registers PREST1- or PREST2, faulty values may be written into the counter registers.
- If the PRESET signal is active or was active up to 40 ms before, the register NONOFFS shall not be written via the serial interface. Otherwise, faulty values may be written to the EEPROM.
- Please pay attention to the maximum number of write cycles for the EEPROM when using the commands WCFG and the PRESET signal.

7.11 Power saving options

To lower the current consumption of the GC-NIP, several functions of the IC can be disabled:

Table 33: Power saving options

Configuration bit	Effect	Typical Application
`CFG2/DISMON` = 1	The pins SMON1, SMON2, CMON1 and CMON2 are inactive.	Adjustment of the analog signals has been finished. These pins are not required for operation of the GC-NIP.
`CFG2/DISV0` = 1	The pins V01 and V02 are inactive.	The mean voltages of the GC-NIP are not used for the sensor (i.e. for measuring bridges).
`CFG3/DISCH2` = 01	ABZ output[1] and counter value of channel 2 is not calculated. The phase angle value of channel 2 is calculated.	GC-NIP is used for nonius calculation.
`CFG3/DISCH2` = 11	Nonius position, phase angle, ABZ output[1] and counter value of channel 2 are not calculated.	GC-NIP is used as one channel interpolator.
`CFG3/DISZ1` = 1	The reference point processing on channel 1 is deactivated.	GC-NIP is used for nonius calculation or as interpolator for measuring scales without reference mark.
`CFG3/DISZ2` = 1	The reference point processing on channel 2 is deactivated.	GC-NIP is used for nonius calculation. GC-NIP is used as interpolator for measuring scales without reference mark. GC-NIP is used as one channel interpolator.

[1] The ABZ output is de-/activated after reset of the IC.

7.12 Signal propagation time

The propagation delay of the input signals through the instrumentation amplifier of the GC-NIP is given by the chosen gain factor and the setting of the cut-off-frequency of the low-pass-filter. The following table shows approximate values for some configurations.

Table 34: Propagation delay analog (td_{ANA})

Configuration	Min	Typ.	Max
CFG1/CFGAF = 00 (150 kHz)	720 ns	800 ns	880 ns
CFG1/CFGAF = 01 (75 kHz)	1,0 µs	1,2 µs	1,4 µs
CFG1/CFGAF = 10 (10 kHz)	2,1 µs	2,4 µs	2,7 µs
CFG1/ CFGAF = 11 (inactive) CFG1/CVGGAIN = 00	70 ns	100 ns	120 ns
CFG2/LP CFGAF = 11 (inactive) CFG1/CVGGAIN = 11	70 ns	130 ns	180 ns

The propagation delay td_{DIG} between sampling and measurement value in the registers `MVAL`, `POSIT` or `CNT1`, `CNT2` as well as at the pins ABZ depends on the selected operating mode:

Table 35: Propagation delay digital (td_{DIG})

Mode	Configuration	Register CNT1/2	Register POSIT	ABZ
Nonius	CFG1/Mode = X000 CFGBiSS/STSEL = 00	112 clock cycles f_{OSZ} 4.3µs @ f_{OSZ} = 26MHz	181 clock cycles f_{OSZ} 7µs @ f_{OSZ} = 26MHz	208 clock cycles f_{OSZ} 8µs @ f_{OSZ} = 26MHz
Two channel	CFG1/Mode = X000 CFGBiSS/ STSEL ≠ 00	112 clock cycles f_{OSZ} 4.3µs @ f_{OSZ} = 26MHz	115 clock cycles f_{OSZ} 4.4µs @ f_{OSZ} = 26MHz	208 clock cycles f_{OSZ} 8µs @ f_{OSZ} = 26MHz

ⓘ *Please note that the **constant** propagation delay of the IC (as in every digital system) causes a frequency dependent phase shift between the analog input signals and the output signals of $\varphi = 2\pi \cdot f \cdot td$. The following figures show this behaviour for the output signal `Z` for two different input signal frequencies as an example. The behaviour of the signals `A` and `B` is equivalent.*

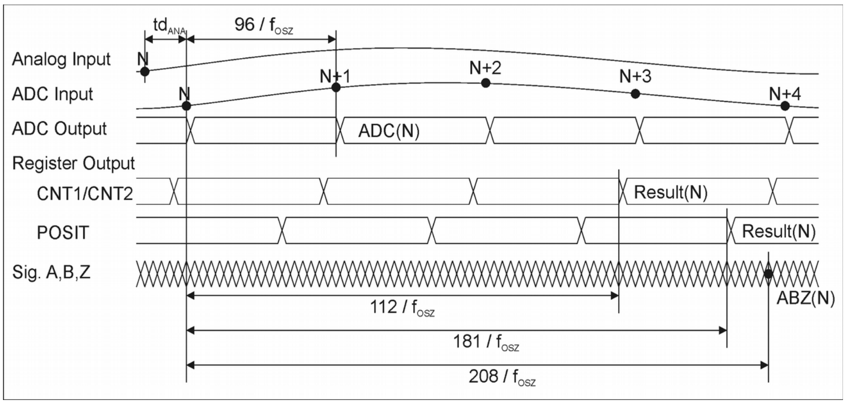


Figure 14: Signal propagation time

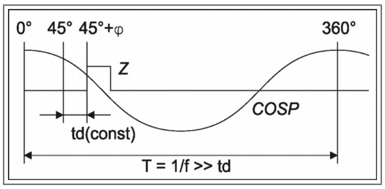


Figure 15: Constant propagation delay

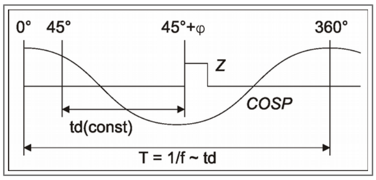


Figure 16: Constant propagation delay

8 Digital interfaces

8.1 Serial interface SPI

The serial interface SPI of the GC-NIP is activated if the pin `SEN` is held on H-level during reset of the IC. The GC-NIP operates in slave mode. In other words: It cannot start communication itself. Up to sixteen ICs can be operated on a single interface bus. The interface is compatible to the most important microcontroller families in SPI mode 0 (16 bit data, MSB first, SCK default low, sampling with rising clock signal edge).

8.1.1 Signals

Signal	Meaning	Direction
SCK	Clock cycle The data at `MOSI` is sampled by the IC with the rising edge at `SCK`. The data at `MISO` is modified by the IC with the falling edge at `SCK`.	IN
SEN	Enable Low: Interface is enabled High: Interface is disabled, `MISO` becomes high-resistant or is set to `nWAIT` Rising edge: Command is executed	IN
MOSI	Master-OUT / Slave-IN Data input	IN
`MISO/nWAIT`	Master-IN / Slave-OUT Data output and status signal Please note: A Pull-Up resistor is required at this pin!	OUT (tristate-capable)

While the IC is reset or during the waiting time of a synchronous SPI read command, the `MISO` line is kept at L level (meaning of `nWAIT`).

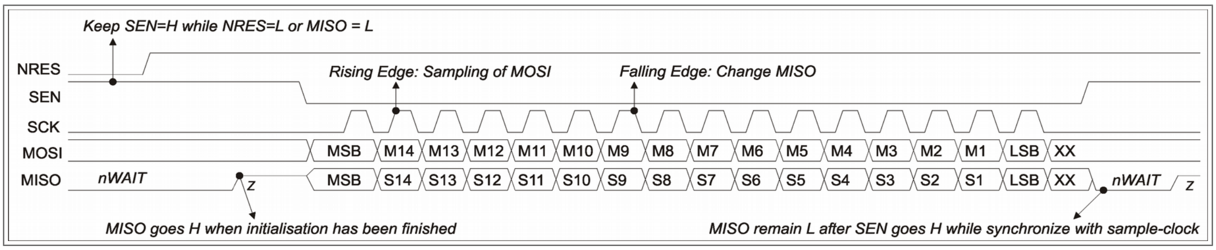


Figure 17: SPI-transfer (1)

8.1.2 Protocol

OP-Code	Description	Bit at signal MOSI															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		OPC				HWA				DATA							
WRA	Write address	1	0	0	nB	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	A1	A0
WRD	Write data	1	0	1	nB	H3	H2	H1	H0	D7	D6	D5	D4	D3	D2	D1	D0
RD0/ST	Read Bytes 0+1 (2 LSB)	1	1	0	X	H3	H2	H1	H0	A7	A6	A5	A4	A3	A2	A1 *)	0
RD1	Read Bytes 2+3 (2 MSB)	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
NOP	Output read register	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

`H(3:0)`: Hardware address, default: '0000', Is not evaluated if `nB` = 0
`A(7:0)`: Register address within an IC
`D(7:0)`: Data word / write data (read data will appear at the pin `MISO`)
`nB`: Broadcast (L-active) 0: Command to all ICs
1: Command to the IC addressed by way of `H(3:0)`

Default-OP-Codes

```
WRA = 0x8000+address     WRD = 0xA000+data
RD0 = 0xC000+address     RD1 = 0xE000
NOP = 0x0000
```

*) Some registers can be addressed for reading 16 bit values. Usually the command `RD0` has to be sent with `A1` set to 0 for reading of the registers.

Any data transfer is initiated by the host processor sending of an SPI word. An SPI word consists of 4 bits OP code, 4 bits hardware address and up to 8 bits data. OP codes are only accepted if the hardware address sent coincides with the hardware address of the GC-NIP. The hardware address of the IC after a reset is '0000'. The command `SETHWA` (see section 9, register `CMD`) can be used to read the pins `HWA<3:0>` into the IC as the new hardware address. OP codes for reading of a register result in data output at the pin `MISO` in the subsequent SPI access (regardless of the hardware address in the new SPI word).

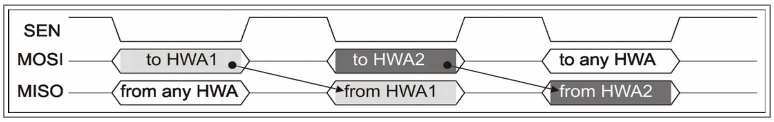


Figure 18: SPI transfer (2)

8.1.3 Register access

Register access in the GC-NIP is done by writing 8 bit and reading 16 bit. The registers of the IC are organized by way of 32 bit blocks. Therefore, the IC contains a 32 bit holding register for read access. Data to be read is stored in the holding register using the SPI word `RD0/ST`. The two least significant bytes of the data to be read is output at the pin `MISO` during the **next** SPI access (see Figure 20). The two most significant bytes of the read access are output with the SPI cycle following the command `RD1`. To read a 32 bit register, the commands `RD0/ST`, `RD1` and `NOP` are usually executed one after another. To read several registers in succession, the sequence `RD0` – `RD1` – `RD0` – `RD1`... can be used (see Figure 22).

To write a GC-NIP register, first the register address must be set using the SPI word `WRA`. Subsequently, the register can be programmed using `WRD`. The register is programmed byte by byte (see Figure 21).

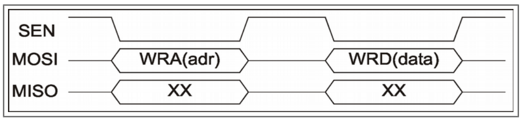


Figure 19: Write access 8 Bit

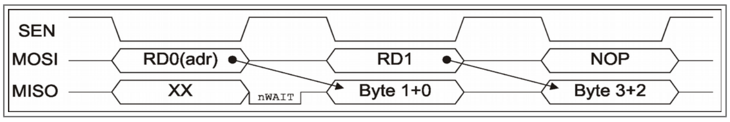


Figure 20: Read access 32 Bit

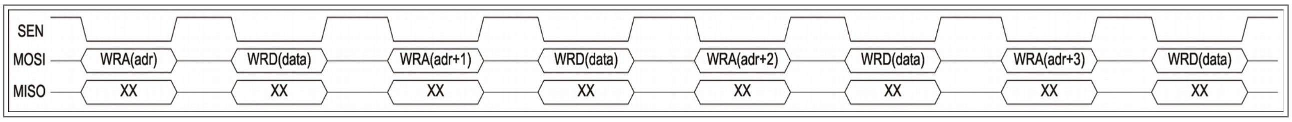


Figure 21: Write access 32 Bit

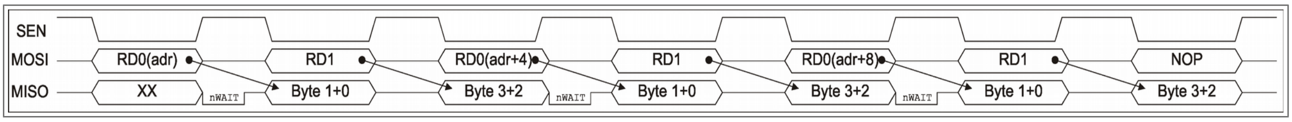


Figure 22: Read access 3 x 32 Bit

8.1.4 Synchronous / asynchronous access

Reading a register, the data is taken over into the holding register synchronously to the internal IC sequence. The value `SYNC` in the register `CFG2` can be used to shift the time relative to the sampling time of the A/D converter. Thus, it is possible to carry out equidistant measurements with small delays.

The pin `MISO` is low during the waiting time (`nWAIT`). If the bit `ASYNC` in the register `CFG2` is set, the data is stored immediately after the rising edge at the signal `SEN`. The time reference to the sampling of the analog signals will be lost. Thus, higher baud rates are achieved.

ⓘ To read the registers `IP11`, `IP12`, `IP21`, `IP22`, `Nonius` or for read access at SPI page 1, a value SYNC(6:0) = 64 (decimal) must be used.

8.2 BiSS interface

The BiSS C-mode interface of the GC-NIP is activated if the pin `SEN` is held on L-level during reset of the IC and the bit `SSI` in register `CFGBISS` is set to '0'. Please note that the level at the pins HWA(3:0) is read in for use as the 4 LSB of the BiSS serial number. Thus multiple ICs can be used on a single interface bus.

For use of the BiSS interface, the integrated EEPROM must contain a valid configuration, because essential operating parameters are stored in EEPROM. The configuration bits `BISSTO` and `READ32` in register `CFGBISS` can be used to adapt the interface to the system parameters.

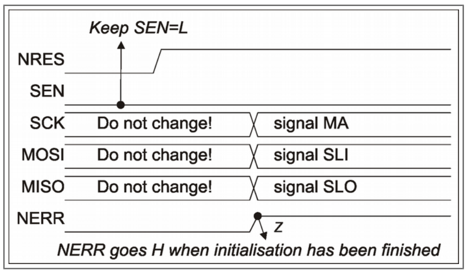


Figure 23: BiSS interface initialization

The Single Cycle Data (SCD) transferred in BiSS C-mode contains the actual position value from register `POSIT` (see section 7.8) with an overall length of 40 bit. This includes the 32 bit position (see table 26), two bits of error information (error and warning bit) and the CRC checksum (polynomial 0x43, 6 bit, inverted).

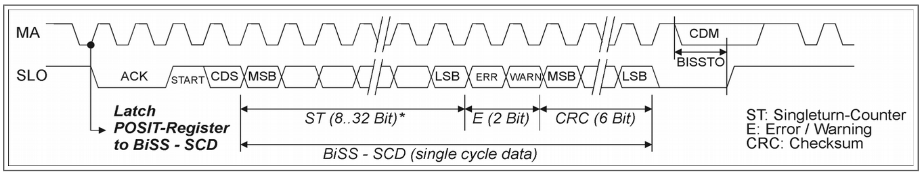


Figure 24: BiSS SCD (Single Data)

Using the BiSS register access, all registers of the GC-NIP are attainable. Reading of 32 bit registers requires the bit `READ32` in register `CFGBISS` to be set. Read access is then handled in 32 bit format, so 4 subsequent addresses, beginning with the least significant address (divisible by 4), must be read by the master. Additionally, the hints for configuring the bits `SYNC(6:0)` of register `CFG2` must be taken into account (see section 8.1.4).

Table 36: Register CFGBISS (BiSS mode)

Bit	Meaning	Vendor configuration	User configuration
BISSTO	BiSS-Timeout	19,7µs at 26 MHz	BISSTO = $\log_2(\text{Timeout}\cdot f_{OSZ})$
READ32	Data format read access	Reading of configuration registers	Reading of data- or configuration registers

Table 37: Default values BiSS register

Register	Vendor configuration	User configuration
BiSS serial number	MSB: 0 LSB: level at pins `HWA(3:0)`	MSB: unique serial number LSB: level at pins `HWA(3:0)`
BiSS Vendor ID	0x47 0x43 („GC“)	User defined ID
BiSS Device ID	0x32 0x03 0x00 0x00	User defined ID
BiSS-Profile + Electronic data sheet (EDS)	unused	User profile

Further specification of the BiSS interface, signal waveforms, register description as well as information to the electronic data sheet (EDS) can be found on the website www.biss-interface.com.

8.3 SSI interface

The SSI interface of the GC-NIP is activated if the pin `SEN` is held on L-level during reset of the IC and the bit `SSI` in register `CFGBISS` is set to '1'. For use of the SSI interface, the integrated EEPROM must contain a valid configuration, because essential operating parameters are stored in EEPROM. The configuration bits `SSITO` and `RING` in register `CFGBISS` can be used to adapt the interface to the system parameters.

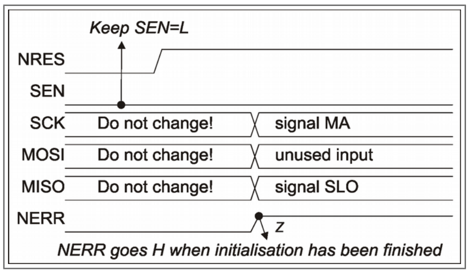


Figure 25: SSI initialization

The SSI data output contains the position value (register `POSIT`, see section 7.8) with an overall length of 20 or 32 bit. This contains the measured position and two bits of error information (error and warning). Setting the bit `RING` in register `CFGBISS` enables continuous transmission of the measurement value in SSI ring mode.

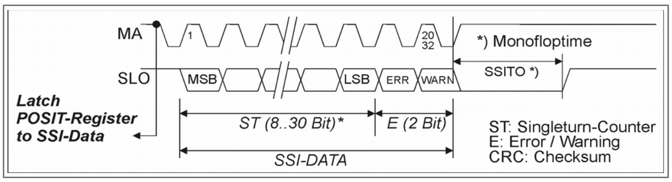


Figure 26: SSI

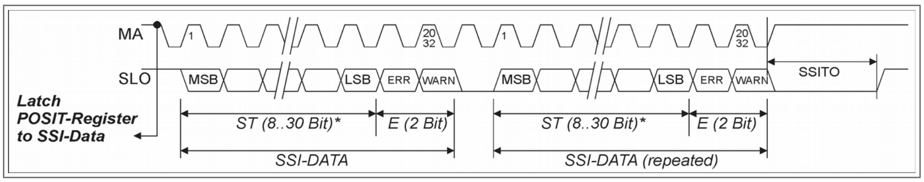


Figure 27: SSI (ring mode)

Table 38: Register CFGBISS (SSI-Mode)

Bit	Meaning	Vendor configuration	User configuration
SSITO	SSI-Timeout		SSITO = (Timeout·f_{OSZ})-3
RING	SSI ring mode	Ring mode	Adapt the operating mode to the master.
SSI20	Output data length	20 bit	0 for 32 bit / 1 for 20 bit

8.4 Simple SPI Master

Setting the Bit CFG1/MODE(3), enables the SPI-master at the pins A, B, Z of channel 2 which sends the position data (register POSIT) cyclical to a connected slave. Additionally, the received data of this SPI form the bits 31:0 of the SSI- or BiSS-data. This way, additional information, for example from an external multiturn counter, can be added to the measurement value or extra error information can be transferred to a control. The microcontroller connected to the SPI must be able to send and receive 32 bits of data with an SPI clock of $f_{OSZ}/2$. It operates in SPI mode 0 (MSB first, sampling on the rising clock edge, clock default low). The following figures show the flow of data and the operational sequence in GC-NIP and in the microcontroller.

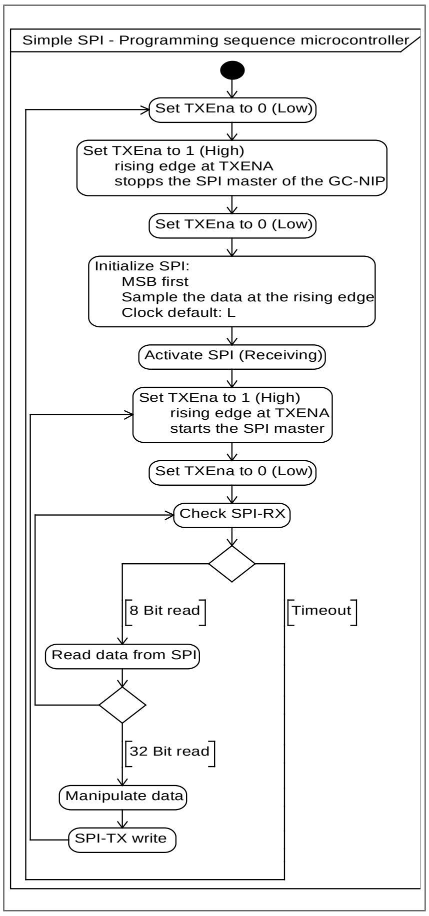


Figure 28: Program sequence microcontroller

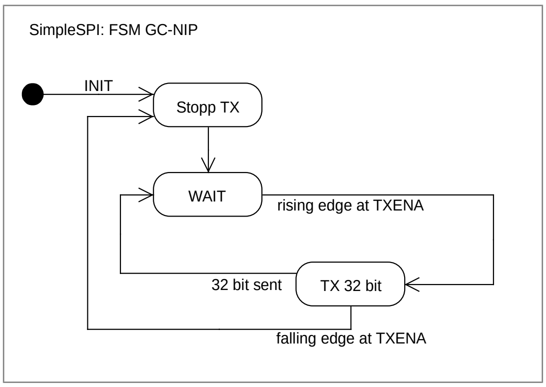


Figure 29: Program sequence GC-NIP

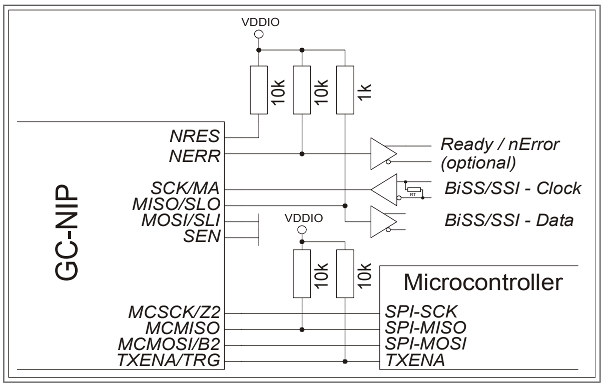


Figure 30: Simple SPI Master

8.5 EEPROM

The GC-NIP contains an integrated EEPROM for permanent storage of the user configuration. The IC checks during reset, if the EEPROM content is valid and sets the configuration. **For validation of the different areas, the EEPROM contains the identifier 0x134A at the EEPROM addresses 0x00-0x02.** Reading from and writing to the EEPROM is handled by an internal interface, which can be accessed using the register `EEP`.

Using the BiSS interface, read access to the EEPROM can be done directly using the BiSS address (40). The address allocation in the EEPROM differs from the addressing via the SPI or BiSS interface.

Table 39: EEPROM addressing

	Register	EEPROM
Word size data	8 Bit	16 Bit
Word size address	8 Bit / 2 Pages	8 Bit / EEPROM address = Register-address / 2
Endianness (user register)	Little Endian	Little Endian or special format
Endianness (BiSS register)	Big Endian	Big Endian

Table 40: Address mapping

Area	Usage	Address SPI	Address BiSS	Address EEPROM	Format
User register	Config	0x00…0x3F (Page 0)	0x00…0x3F (Page 0)	0x00 … 0x1F	Little Endian
BiSS register	BiSS	-	0x40…0x47	0x20 … 0x23	Big Endian
User register	Special	0x48…0x77 (Page 0)	0x48…0x77	0x24 … 0x3B	Little Endian
BiSS register	BiSS	-	0x78…0x7F	0x3C … 0x3F	Big Endian
BiSS EDS-Common	BiSS	-	0x00…0x3F (Page 1)	0x40 … 0x5F	Big Endian
BiSS EDS-Profile 1	BiSS	-	0x00…0x3F (Page 2)	0x60 … 0x7F	Big Endian
BiSS EDS-Profile 2	BiSS	-	0x00…0x3F (Page 3)	0xC0 … 0xDF	Big Endian
User register	Coefficients	0x40…0x7F (Page 1)	0x00…0x3F (Page 4)	0xA0 … 0xBF	Little Endian
User register	IP-Table	0x80…0xBF (Page 1)	0x00…0x3F (Page 5)	0x80 … 0x9F	Special format 20 bit
User register	IP-Table (fix)		0x00…0x3F (Page 6)	0xE0 … 0xFF	Special format 20 bit
User register	Read-Register	0x80…0xBF (Page 0)	0x00…0x3F (Page 7)	-	Little Endian
Page register SPI	Page	0xFF (any Page)	-	-	Byte

The sequence for reading and writing the EEPROM are described in section 11.4. It is important to ensure not to write the EEP register if the bit EEPBSY in register EEP is set.

9 Register

Table 41: Register overview

Register	Access 1)	Address SPI	BiSS-Page	Address BiSS	Address EEPROM 2)	Hints
IDREV + Status	R	0x00	0	0x00...0x03	0x00...0x01	0x00: valid flag for configuration
CFGEEP	!	0x04...0x07		0x04...0x07	0x02...0x03	0x01: valid flag for the coefficients
CFG1	RW	0x08...0x0B		0x08...0x0B	0x04...0x05	
CFG2	RW	0x0C...0x0F		0x0C...0x0F	0x06...0x07	
CFG3	RW	0x10...0x13		0x10...0x13	0x08...0x09	
Unused	RW	0x14...0x17		0x14...0x17	0x0A...0x0B	
Unused	RW	0x18...0x1B		0x18...0x1B	0x0C...0x0D	
CTRLG1	RW	0x1C...0x1F		0x1C...0x1F	0x0E...0x0F	
CTRLO1	RW	0x20...0x23		0x20...0x23	0x10...0x11	
PREST1	RW	0x24...0x27		0x24...0x27	0x12...0x13	
CTRLG2	RW	0x28...0x2B		0x28...0x2B	0x14...0x15	
CTRLO2	RW	0x2C...0x2F		0x2C...0x2F	0x16...0x17	
PREST2	RW	0x30...0x33		0x30...0x33	0x18...0x19	
NONOFFS	RW	0x34...0x37		0x34...0x37	0x1A...0x1B	Change EEP at Preset signal / no update at cmd WCFG
CFGBISS	RW	0x38...0x3B		0x38...0x3B	0x1C...0x1D	No update at cmd WCFG
CFGGEMAC	!	0x3C...0x3F		0x3C...0x3F	0x1E...0x1F	No update at cmd WCFG /write protect
BiSS-PAGE	RW	-	-	0x40		SPI-Page
BiSS-EDS-Bank	R (EEP)	-		0x41	0x20 (MSB)	
BiSS-Profile	R (EEP)	-		0x42...0x43	0x21	
BiSS-Serial-Number	R (EEP)	-		0x44...0x47	0x22 ... 0x23	
EEP_DAT	RW	0x48...0x49		0x48...0x49		
EEP_ADR / EEP_STAT	W / R	0x4A		0x4A		
EEP_OPC / EEP_MSB	W	0x4B		0x4B		
CFGTM	RW	0x4C..0x4F		0x4C...0x4F		
CMD (16 Bit)	W	0x50...0x51		0x50...0x52		
TSTCMD (16 Bit)	W	0x52...0x53		0x52...0x53		Write protected
Unused	RW / !	0x54...0x67		0x54...0x67		
Adjust3	!	0x68...0x6B		0x68...0x6B	0x34...0x35	Write protected
Adjust2	!	0x6C...0x6F		0x6C...0x6F	0x36...0x37	
Adjust1	!	0x70...0x73		0x70...0x73	0x38...0x39	
Adjust0	!	0x74...0x77		0x74...0x75	0x3A...0x3B	
BiSS-Device-Identifier	R (EEP)	-		0x78...0x7B	0x3C...0x3D	
BISS-Timeout	RW	-		0x7C...0x7D	0x3E	
BiSS-Vendor-Identifier	R (EEP)	-		0x7E...0x7F	0x3F	
EDS-Common	R (EEP)	-	1	0x00...0x3F	0x40...0x5F	
EDS-Profil 1	R (EEP)	-	2	0x00...0x3F	0x60...0x7F	
EDS-Profil 2	R (EEP)	-	3	0x00...0x3F	0x80...0x9F	
Coefficients	R (SPI1)	0x40...0x7F	4	0x00...0x3F	0xA0...0xBF	
IP-Table	R (SPI1)	0x80...0xBF	5	0x00...0x3F	0xC0...0xDF	
IP-Table (fix)			6	0x00...0x3F	0xE0...0xFF	Write protected
MVAL		0x80	7	0x00...0x03		
CNT1		0x84		0x04...0x07		
POSIT		0x88		0x08...0x0B		
ADC1		0x8C		0x0C...0x0F		
CADC1		0x90		0x10...0x13		
IP11		0x94		0x14...0x17		
IP21		0x98		0x18...0x1B		
IP3		0x9C		0x1C...0x1F		
Unused		0xA0		0x20...0x23		
CNT2		0xA4		0x24...0x27		
Unused		0xA8		0x28...0x2B		
ADC 2		0xAC		0x2C...0x2F		
CADC2		0xB0		0x30...0x33		
IP12		0xB4		0x34...0x37		
IP22		0xB8		0x38...0x3C		
NONIUS		0xBC		0x3C...0x3F		
SPI-Page = SPI-MSB	RW	0xFF	-	-	-	Any SPI-Page

1) R: Read only (register 32 Bit) W: Write only (register) RW: Read/Write (register) R (EEP): Read only (EEPROM via BiSS)
R (SPI): Read only via SPI-Page 1 !: Vendor register. shall/can not be changed!

2) The EEPROM address is used for the internal EEPROM interface (register `EEP`).

dark gray : This register is loaded from EEPROM during reset
blue: BiSS-Information, direct read from EEPROM
white: EEPROM contains the valid identifier 0x134A

CNT1	***Counter value (Interpolation counter) channel 1***
CNT2	***Counter value (Interpolation counter) channel 2***

31:2	1	0
CNT	ZSTAT	ERR

Bit	Name	Reset value	Format	Value	Meaning
31:2	CNT	0x0000	Signed		Counter value
1	ZSTAT	0	Bit	0	The reference mark (index) of the scale has not yet been passed or the reference of count value and reference mark was lost due to an error.
				1	The reference mark (index) of the scale has been passed; GC-NIP and scale operate synchronously.
0	ERR	0	Bit	0	Measured value is valid.
				1	An error occurred. The current measurement value and all subsequent values are to be discarded. After rectification of the error cause and resetting of the error bits (command `RESCNT` or `PRESET` pulse) it is imperative to pass through the reference point to be able to perform further absolute measurements.

POSIT	***Position data (also: BiSS/SSI-SCD)***

31:17	16:2	1	0
NONIUS		ERR	WARN
CNT1		ERR	WARN
CNT2		ERR	WARN
CNT2	CNT1	ERR	WARN

Bit	Name	Reset value	Format	Value	Meaning
31:2	NONIUS	0x0000	Unsigned (optional: Gray)		`CFGBISS/STSEL(1:0)` = `00` Absolute position calculated by the nonius method. The data format is selected by `CFGBISS/GRAY`.
	CNT1	0x0000	Signed (optional Gray)		`CFGBISS/STSEL(1:0)` = `01` Counter value of channel 1. The data format is selected by `CFGBISS/GRAY`.
	CNT2	0x0000	Signed (optional Gray)		`CFGBISS/STSEL(1:0)` = `10` Counter value of channel 2. The data format is selected by `CFGBISS/GRAY`.
	CNT1 CNT2	0x0000	Signed 15 Bit		`CFGBISS/STSEL(1:0)` = `11` Counter value of channel 1 and channel 2 (15 bit each). `CFGBISS/GRAY` should be 0.
1	ERR	0	Bit	0	Measured value is valid.
				1	An error occurred. The current measurement value and all subsequent values are to be discarded. After rectification of the error cause and resetting of the error bits (command `RESCNT` or `PRESET` pulse) it is imperative to pass through the reference point to be able to perform further absolute measurements.
0	WARN	0	Bit	0	Measured value is valid.
				1	The measured value has a limited accuracy.

MVAL	**Measured value / trigger value**

31:2	1	0
POSIT/TVAL	TRG	ERR

Bit	Name	Reset value	Format	Value	Meaning
31:2	POSIT/ TVAL	0x0000	→ `POSIT`		Measured value; value corresponds to register POSIT or contents of a trigger holding register. A trigger holding register may be freed by reading this register. → see sections 7.7, 7.8
1	TRG	0	Bit	0	Measured value corresponds to content of register `POSIT`.
				1	Measured value corresponds to contents of a trigger holding register.
0	ERR	0	Bit	0	Measured value is valid.
				1	An error occurred. The current measurement value and all subsequent values are to be discarded. After rectification of the error cause and resetting of the error bits (command `RESCNT` or `PRESET` pulse) it is imperative to pass through the reference point to be able to perform further absolute measurements.

STAT / ID / REV	**ASIC identifier / status**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ASICID				ASICREV				ENON	TRGOVL	TRGZ	TRG	ZSTAT2	ZSTAT1	ESOFF2	ECOFF2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ESGAIN2	ECGAIN2	EABZ2	EFAST2	ESADC2	ECADC2	EVLOW2	ESOFF1	ECOFF1	ESGAIN1	ECGAIN1	EABZ1	EFAST1	ESADC1	ECADC1	EVLOW1

Bit	Name	Reset value	Format	Value	Meaning
31:28	ASICID	0011	Binary	0011	The IC is a GC-NIP
27:24	ASICREV	10	Binary		Silicon revision of the IC
23	ENON	0	Bit	0	No error in calculation of the nonius value. Measurement value is plausible.
				1	The calculated absolute position is invalid. Cause are either errors of the input signals, which can not be internally corrected, or unfavourable combinations of the correction coefficients stored in the EEPROM. The nonius sensor shall be calibrated.
22	TRGOVL	0	Bit	0	No overflow of the trigger holding register.
				1	Overflow of the trigger holding register; trigger event was lost.
21	TRGZ	0	Bit	0	Next measured value read from register `MVAL` was not triggered by the reference signal.
				1	Next measured value read from register `MVAL` was triggered by the reference signal.
20	TRG	0	Bit	0	Next measured value read from register `MVAL` was not triggered by the pin `TRG`.
				1	Next measured value read from register `MVAL` was triggered by the pin `TRG`.
19	ZSTAT2	0	Bit	0	The reference mark (channel 2) of the scale has not yet been passed or the reference of count value and reference mark was lost due to an error.
				1	The reference mark (channel 2) of the scale has been passed. Counter and scale operate synchronously.
18	ZSTAT1	0	Bit	0	The reference mark (channel 1) of the scale has not yet been passed or the reference of count value and reference mark was lost due to an error.
				1	The reference mark (channel 1) of the scale has been passed. Counter and scale operate synchronously.
17	ESOFF2	0	Bit	0	No offset error at sinusoidal signal at channel 2
				1	The offset controller for the sinusoidal signal has reached its limit. The cause is an excessive signal offset, a partly of fully disconnected sensor on an invalid value for initialization of the controller.
16	ECOFF2	0	Bit	0	No offset error at cosinusoidal signal at channel 2
				1	The offset controller for the cosinusoidal signal has reached its limit. The cause is an excessive signal offset, a partly of fully disconnected sensor on an invalid value for initialization of the controller.
15	ESGAIN2	0	Bit	0	No amplitude error at sinusoidal signal at channel 2
				1	The gain controller for the sinusoidal signal has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.

Bit	Name	Reset value	Format	Value	Meaning
14	ECGAIN2	0	Bit	0	No amplitude error at sinusoidal signal at channel 2
				1	The gain controller for the cosinusoidal signal has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.
13	EABZ2	0	Bit	0	No error at A,B,Z channel 2
				1	The signals `A`, `B` and `Z` are invalid. The cause is an excessive input frequency. The monitored frequency depends on the set minimum edge interval t_{pp}. This error also occurs if the interpolation rate or the minimum edge interval is changed. Detection of this error is deactivated for the counter mode.
12	EFAST2	0	Bit	0	No speed error at channel 2
				1	The input frequency is so high that no A/B signals can be generated or the direction can no longer be detected. The monitored frequency is different depending on whether an internal counter or the square-wave outputs A/B/Z are used.
11	ESADC2	0	Bit	0	No ADC error at the sinusoidal signal at channel 2
				1	The A/D converter for the sinusoidal signal is overdriven. The cause is that the signal amplitude is too high. This error may also occur with signals with very large offset at simultaneously high amplitude.
10	ECADC2	0	Bit	0	No ADC error at the cosinusoidal signal at channel 2
				1	The A/D converter for the cosinusoidal signal at is overdriven. The cause is that the signal amplitude is too high. This error may also occur with signals with very large offset at simultaneously high amplitude.
9	EVLOW2	0	Bit	0	No vector error at channel 2
				1	The signal vector generated from the sinusoidal and cosinusoidal signals is too small. Usually, the cause is a partly or completely disconnected sensor. This error may also occur with signals with very large offset at simultaneously low amplitude.
8	ESOFF1	0	Bit	0	No offset error at sinusoidal signal at channel 1
				1	The offset controller for the sinusoidal signal has reached its limit. The cause is an excessive signal offset, a partly of fully disconnected sensor on an invalid value for initialization of the controller.
7	ECOFF1	0	Bit	0	No offset error at sinusoidal signal at channel 1
				1	The offset controller for the cosinusoidal signal has reached its limit. The cause is an excessive signal offset, a partly of fully disconnected sensor on an invalid value for initialization of the controller.
6	ESGAIN1	0	Bit	0	No amplitude error at sinusoidal signal at channel 1
				1	The gain controller for the sinusoidal signal has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.
5	ECGAIN1	0	Bit	0	No amplitude error at sinusoidal signal at channel 1
				1	The gain controller for the cosinusoidal signal has reached its limit. The cause is either that the signal amplitude is too low or the sensor is partly or fully disconnected.
4	EABZ1	0	Bit	0	No error at A,B,Z channel 1
				1	The signals `A`, `B` and `Z` are invalid. The cause is an excessive input frequency. The monitored frequency depends on the set minimum edge interval t_{pp}. This error also occurs if the interpolation rate or the minimum edge interval is changed. Detection of this error is deactivated for the counter mode.
3	EFAST1	0	Bit	0	No speed error at channel 1
				1	The input frequency is so high that no A/B signals can be generated or the direction can no longer be detected. The monitored frequency is different depending on whether an internal counter or the square-wave outputs A/B/Z are used.
2	ESADC1	0	Bit	0	No ADC error at the sinusoidal signal at channel 1
				1	The A/D converter for the sinusoidal signal is overdriven. The cause is that the signal amplitude is too high. This error may also occur with signals with very large offset at simultaneously high amplitude.
1	ECADC1	0	Bit	0	No ADC error at the sinusoidal signal at channel 1
				1	The A/D converter for the cosinusoidal signal is overdriven. The cause is that the signal amplitude is too high. This error may also occur with signals with very large offset at simultaneously high amplitude.
0	EVLOW1	0	Bit	0	No vector error at channel 1
				1	The signal vector generated from the sinusoidal and cosinusoidal signals is too small. Usually, the cause is a partly or completely disconnected sensor. This error may also occur with signals with very large offset at simultaneously low amplitude.

CMD Command

7	6	5	4	3	2	1	0
TRGCAL	PRESET	SETHWA	WCFG	RESIC	CLRZ	RESCTL	RESCNT

Bit	Name	Reset value	Format	Value	Meaning
7	TRGCAL		Bit write-only	1	The registers used for calibration are refreshed. Also, the registers are refreshed if the trigger (Pin `TRG`) is active.
6	PRESET		Bit write-only	1	The offset for the nonius position `NONOFFS` is re-calculated using the preset value for the nonius from register PREST2 and the new offset value (`NONOFFS`) is stored in the EEPROM. The bit `CFG2/PREENA` has to be set for this function.
5	SETHWA		Bit write-only	1	The pins `HWA3`, `HWA2`, `HWA1` and `HWA0` are read into the IC as hardware addresses. If several ICs are to be connected to one SPI interface, this command must be sent first to all connected ICs. This command is automatically set during initialization if the BiSS interface is activated.
4	WCFG		Bit write-only	1	The content of the registers `CFG1`, `CFG2`, `CFG3`, `CNTRLG`, `CNTRLO`, `PREST1` and `PREST2` are transferred to the EEPROM.
3	RESIC		Bit write-only	1	The IC is reset and re-configured.
2	CLRZ		Bit write-only	1	The status bit `ZSTAT` is reset. For the trigger modes “Adjustment Z” and “Distance coded” this command starts a new measurement (see 7.7).
1	RESCTL		Bit write-only	1	The internal controller for gain and offset is reset, i.e. all correction values for offset and gain are set to the center of their value range.
0	RESCNT		Bit write-only	1	The counter values (`CNT1`/`CNT2`) are set to the value in the registers `PREST1`/`PREST2`. All error flags in the status register are reset and the bit `ZSTAT` is reset. For the trigger modes “Adjustment Z” and “Distance coded” this command starts a new measurement (see 7.7).

CFG1 Configuration 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRI	LNON	LOFF	LGAIN	LABZ	LFAST	LADC	LVLOW	HLD	MNON	MOFF	MGAIN	MABZ	MFAST	MADC	MVLOW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GAIN		CFGAF		MODE				CFGTPP			TRGSLP	IRMAP	IRD2SEL	IRDIV1	

Bit	Name	Reset value	Format	Value	Meaning
31	TRI	0	Bit	0	The behaviour of the signals `A,B` and `Z` is determined by bit `HLD` in case of error.
				1	The signals `A,B` and `Z` are high resistant in case of error.
30	LNON	0	Bit	0	Detected nonius errors (ENON) are not saved.
				1	Detected nonius errors (ENON) are saved.
29	LOFF	0	Bit	0	Detected offset errors (EOFF) are not saved.
				1	Detected offset errors (EOFF) are saved.
28	LGAIN	0	Bit	0	Detected gain errors (EGAIN) are not saved.
				1	Detected gain errors (EGAIN) are saved.
27	LABZ	0	Bit	0	Detected A/B/Z errors (EABZ) are not saved.
				1	Detected A/B/Z errors (EABZ) are saved.
26	LFAST	0	Bit	0	Detected speed errors (EFAST) are not saved.
				1	Detected speed errors (EFAST) are saved.
25	LADC	0	Bit	0	Detected ADC errors (EADC) are not saved.
				1	Detected ADC errors (EADC) are saved.
24	LVLOW	0	Bit	0	Detected vector errors (ELVLOW) are not saved.
				1	Detected vector errors (ELVLOW) are saved.
23	HLD	1	Bit	0	The behaviour of the signals `A,B` and `Z` is not defined in case of error.
				1	The signals `A,B` and `Z` do not change in case of error.
22	MNON	1	Bit	0	The detection of nonius errors (ENON) is deactivated.
				1	The detection of nonius errors (ENON) is activated.
21	MOFF	1	Bit	0	The detection of offset errors (EOFF) is deactivated.
				1	The detection of offset errors (EOFF) is activated.
20	MGAIN	1	Bit	0	The detection of gain errors (EGAIN) is deactivated.
				1	The detection of gain errors (EGAIN) is activated.
19	MABZ	0 (EEP) 1 (Pin)	Bit	0	The detection of A/B/Z errors (`EABZ`) is deactivated; the IC operates in the counter mode.
				1	The detection of A/B/Z errors (`EABZ`) is activated; the IC operates in the square-wave mode.
18	MFAST	1	Bit	0	The detection of speed errors (`EFAST`) is deactivated.
				1	The detection of speed errors (`EFAST`) is activated.
17	MADC	1	Bit	0	The detection of ADC errors (EADC) is deactivated.
				1	The detection of ADC errors (EADC) is activated.
16	MVLOW	1	Bit	0	The detection of vector errors (ELVLOW) is deactivated.
				1	The detection of vector errors (ELVLOW) is activated.
15:14	GAIN	Pins CFGGAIN	binary	00	Nominal signal amplitude 660 mV_{pp}
				01	Nominal signal amplitude 250 mV_{pp}
				10	Nominal signal amplitude 120 mV_{pp}
				11	Nominal signal amplitude 60 mV_{pp}
13:12	CFGAF	Pins CFGAF	binary	00	Analog low-pass-filter cut-off frequency 150kHz -0.5dB
				01	Analog low-pass-filter cut-off frequency 75kHz -1dB
				10	Analog low-pass-filter cut-off frequency 10kHz -1dB
				11	Analog low-pass-filter inactive
11:8	MODE	0000	binary		Configuration of the output signals and operating mode as per Table 19
7:5	CFGTPP	000	binary	TPP	Configuration of the minimum edge interval t_{pp}; $t_{pp} = 2^{TPP} / f_{OSZ}$
4	TRGSLP	0	Bit	0	A falling edge at pin `TRG` accepts the measured value into the trigger holding register.
				1	A falling edge at pin `TRG` accepts the measured value into the trigger holding register.
3	IRMAP	0 (EEP) 1 (Pin)	Bit	0	Base interpolation rate and nonius pitch are read from EEPROM
				1	Base interpolation rate = 2000, nonius pitch = 125
2	IRD2SEL	0	Bit	0	The divider factor for the interpolation rate of channel 1 and 2 are equal.
				1	The divider factor for the interpolation rate of channel 2 is set by `CFG3/IRDIV2`.
1:0	IRDIV1	00	binary	N	The base interpolation rate (set by `IRMAP`) used for the counter and the A/B output is divided by 2^N.

CFG2 Configuration 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DISMON	DISV0	PH_2						PREENA	PHBER	PH_1					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASYNC	SYNC							ZMODE		Z4	ZPOS				

Bit	Name	Reset value	Format	Value	Meaning
31	DISMON	0	Bit	0	The pins SMON1, SMON2, CMON1 and CMON2 are active.
				1	The pins SMON1, SMON2, CMON1 and CMON2 are inactive (power saving option).
30	DISV0	0	Bit	0	The pins V01, V02 are active.
				1	The pins V01 V02 are inactive (power saving option).
29:24	PH_2	000000	signed	-32	Largest phase displacement negative.
				PH	Setting value of the phase correction potentiometer of channel 2.
				+31	Largest phase displacement positive.
23	PREENA	0	Bit	0	The preset function for calculating a new offset value is inactive.
				1	The preset function for calculating a new offset value is active (see 7.10.1).
22	PHBER	0	Bit	0	The setting range of the phase correction potentiometer is ± 5°. The step size is 0.156°.
				1	The setting range of the phase correction potentiometer is ± 10°. The step size is 0.313°.
21:16	PH_1	000000	signed	-32	Largest phase displacement negative.
				PH	Setting value of the phase correction potentiometer of channel 1.
				+31	Largest phase displacement positive.
15	ASYNC	0	Bit	0	The data to be read are accepted into a 32-bit holding register synchronously to the internal sequence using the SPI word `RD0/ST`. The time of acceptance can be shifted relative to the sampling time using the value of `SYNC`.
				1	Data to be read are accepted asynchronously into a 32-bit holding register using the SPI word `RD0/ST`. The value of `SYNC` is not evaluated.
14:8	SYNC	0000000	unsigned		Displacement of an SPI read access relative to the sampling time. To read the registers `IP11`, `IP12`, `IP21`, `IP22`, `Nonius` and to read at SPI page 1 a value of 64 (dec) must be used.
7:6	ZMODE	00	binary	00	Reference point evaluation mode Incremental
				01	Reference point evaluation mode Trigger
				10	Reference point evaluation mode Adjustment Z
				11	Reference point evaluation mode Distance coded
5	Z4	0	Bit	0	The width of the zero signal `Z` is one increment = ¼ period
				1	The width of the zero signal `Z` is four increments = 1 period
4:0	ZPOS	00100 (45°)	unsigned	ZPOS	Displacement of the reference point position according to the sinusoidal signal at the input. Reference position = ZPOS · 11.25° This register is not used if CFG3/NOSEL = 1 (see section 7.6.3)

CFG3 Configuration 3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	NOSEL	IRDIV2	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISCH2		MXFEED	MXSHR	ZDEL2	ZDEL	DISZ2	DISZ1	DH			OFFSCTL		GAINCTL		DISCTL

Bit	Name	Reset value	Format	Value	Meaning
18	NOSEL	0	Bit	0	The register `NONOFFS` is used for calculation of the absolute position (nonius). The signal `PRESET` causes the re-calculation of the offset value.
				1	The register `NONOFFS` contains the reference point position for channel 1 and channel 2. the signal `PRESET` causes the re-calculation of the reference point positions.
17:16	IRDIV2	00	binary	N	The base interpolation rate (set by `IRMAP`) used for the counter and the A/B output on channel 2 is divided by 2^N, if enabled by `CFG1/IRD2SEL` = 1.
15:14	DISCH2	00	Bit	00	Nonius, phase angle, ABZ outputs[1] and counter of channel 2 are calculated. → Nonius, one channel and two channel operating mode possible.
				01	Counter and ABZ outputs0[1] of channel 2 are not calculated. The phase angle value of channel 2 is calculated. → Nonius and one channel operating mode possible.
				10	invalid
				11	Nonius, phase angle, ABZ outputs[1] and counter of channel 2 are not calculated. → One channel operating mode possible.
13	MXFEED	0	Bit	0	The correction value is calculated from the coefficients stored in EEPROM.
				1	Coefficient 14 is applied as correction value. → One channel and two channel operating mode possible.
12	MXSHR	1	Bit	0	Coefficient scaling 16 Bit
				1	Coefficient scaling 16/18 Bit
11	ZDEL2	0	Bit	0	Default value
				1	Additional internal delay of the reference signal Z of 96/f_{OSZ}.
10	ZDEL	0	Bit	0	Default value
				1	Additional internal delay of the reference signal Z of 96/f_{OSZ}.
9	DISZ2	00	Bit	0	Reference point processing at channel 2 is activated. Activation (DISZ2 changes from 1 to 0) requires a processing time of 100µs.
				1	Reference point processing at channel 2 is deactivated.
8	DISZ1	00	Bit	0	Reference point processing at channel 1 is activated. Activation (DISZ1 changes from 1 to 0) requires a processing time of 100µs
				1	Reference point processing at channel 1 is deactivated.
7:5	DH	01	binary	DH	Threshold value for the digital hysteresis. A value of 0 deactivates the digital hysteresis.
4:3	OFFSCTL	01	binary	00	Maximum settling time for the offset controller. This configuration must be selected if the sensor signal has a lower input frequency or is overlaid by noise, or the phase between sinusoidal and cosinusoidal signals cannot be fully adjusted using the phase correction potentiometer.
				01	Reduction of the settling time of the offset controller by a factor of approx. 2
				10	Reduction of the settling time of the offset controller by a factor of approx. 4
				11	Reduction of the settling time of the offset controller by a factor of approx. 8
2:1	GAINCTL	01	binary	00	Maximum settling time for the gain controller. This configuration must be selected if the sensor signal has a lower input frequency or is overlaid by noise, or the phase between sinusoidal and cosinusoidal signals cannot be fully adjusted using the phase correction potentiometer.
				01	Reduction of the settling time of the gain controller by a factor of approx. 2
				10	Reduction of the settling time of the gain controller by a factor of approx. 4
				11	Reduction of the settling time of the gain controller by a factor of approx. 8
0	DISCTL	0	Bit	0	The internal controller for gain and offset is activated.
				1	The internal controller for gain and offset is deactivated.

[1] The ABZ output is de-/activated after reset of the IC.

CFGBISS	**Configuration SSI and BiSS interface**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SSI	-	SSI20	RING	SSITO(11:0)											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STSEL1	STSEL0	GRAY	STBIT					-	READ32	-	BISSTO(4:0)				

Bit	Name	Reset value	Format	Value	Meaning
31	SSI	1	Bit	0	BiSS is used as digital interface if BiSS/SSI is enabled by `SEN=Low` during reset.
				1	SSI is used as digital interface if BiSS/SSI is enabled by `SEN=Low` during reset.
29	SSI20	1		0	32 Bit SSI-Data
				1	20 Bit SSI-Data
28	RING	1	Bit	0	SSI Ring mode inactive
				1	SSI Ring mode active
27:16	SSITO	517 decimal	unsigned	SSITO	Configuration SSI timeout parameter $\mathtt{Timeout} = (\mathtt{SSITO}+3)/f_{OSZ}$ or $\mathtt{SSITO} = (\mathtt{Timeout} \cdot f_{OSZ})-3$ Example: f_{OSZ} = 26MHz → `SSITO` = 23(1µs) … 517(20µs) … 2047 (79 µs)
15:14	STSEL	00	binary	00	The position value is determined by the nonius calculation.
				01	The counter value of channel 1 is used as position value.
				10	The counter value of channel 2 is used as position value.
				11	For debug purpose only: / the position value contains the counter values of channel 1 and channel 2 with 16 bit each. Gray-coding shall not be used.
13	GRAY	0	Bit	0	The position data is binary coded.
				1	The position data is gray coded.
12:8	STBIT	30 decimal	binary	STBIT	Resolution of the position data in bits; range: 8-30 bit. Unused MSB are filled with zero This value has no effect if `STSEL` = 11.
6	READ32	0	Bit	0	8 bit BiSS read access. Suitable for reading configuration registers.
				1	32 bit BiSS read access. 4 subsequent addresses, beginning with the least significant address (divisible by 4), must be read. Suitable for reading data and user registers.
4:0	BISSTO	9 decimal	unsigned	BISSTO	Configuration of the BiSS-Timeout; values: 12µs....40µs. $\mathtt{Timeout} = 2^{\mathtt{BISSTO}}/f_{OSZ}$ or $\mathtt{BISSTO} = \log2(\mathtt{Timeout} \cdot f_{OSZ})$ Example: f_{OSZ} = 26MHz → `BISSTO` = 9(19.7µs) or 10(39.4µs)

ⓘ This register has to be configured in EEPROM via SPI to ensure correct BiSS functionality.

PREST1	**Preset-Value channel 1**
PREST2	**Preset-Value channel 2 / nonius**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRE(31:16)															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRE(15:0)															

Bit	Name	Reset value	Format	Value	Meaning
31:0	PRE	0	unsigned	PRE	Preload-Value; → see section 7.10

NONOFFS	**Nonius Offset-Value**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OFFS(31:16) ZPOSCH2															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFFS(15:0) ZPOSCH1															

Bit	Name	Reset value	Format	Value	Meaning
31:0	OFFS	0	unsigned	OFFS	Offset value for nonius calculation → see section 7.10
31:16	ZPOSCH2	0	unsigned	ZPOS 0 IRATE-1	Configuration of the reference position referred to the sinusoidal signal. Condition: CFG3/NOSEL = 1 → see section 7.6.3, 7.10.2 Minimum value Maximum value
15:0	ZPOSCH1	0	unsigned		

CNTRLG1	**Controller: Gain correction value channel 1**
CNTRLG2	**Controller: Gain correction value channel 2**

When writing the bits 26:16, the bits 23:16 must be written first. Subsequently, the whole correction value is refreshed in the register by writing of the bits 26:24.
When writing the bits 10:0, the bits 7:0 must be written first. Subsequently, the whole correction value is refreshed in the register by writing of the bits 10:8.
Please not that the correction values are changed automatically by the IC with active signal control.

31	30	29	28	27	26:16
-	-	-	-	-	CNTRLG_S

15	14	13	12	11	10:0
-	-	-	-	-	CNTRLG_C

Bit	Name	Reset value	Format	Value	Meaning
26:16	CNTRLG_S	0x400	unsigned	CNTRLG 0x000 0x400 0x7FF	CADC_S = [ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/2048) CADC_C = [ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/2048) Minimum value; the offset-corrected ADC values of the sinusoidal signal are multiplied by 0.5. Mean value; the offset-corrected ADC values of the sinusoidal signal are multiplied by 1.0. the Maximum value: offset-corrected ADC values of the sinusoidal signal are multiplied by 1.5.
10:0	CNTRLG_C	0x400	unsigned		

CNTRLO1	**Controller: Offset correction value channel 1**
CNTRLO2	**Controller: Offset correction value channel 2**

When writing the bits 31:16, the bits 23:16 must be written first. Subsequently, the whole correction value is refreshed in the register by writing of the bits 31:24. If the value to be written lies outside the valid range of -2730...+2729, the correction register is no longer refreshed, and the bit `ESOFF` in the register `STAT/ERR` is set.
When writing the bits 15:0, the bits 7:0 must be written first. Subsequently, the whole correction value is refreshed in the register by writing of the bits 15:8. If the value to be written lies outside the valid range of -2730...+2729, the correction register is no longer refreshed, and the bit `ECOFF` in the register `STAT/ERR` is set.
Please note that the correction values are changed automatically by the IC with active signal control.

31:16
CNTRLO_S

15:0
CNTRLO_C

Bit	Name	Reset value	Format	Value	Meaning
31:16	CNTRLO_S	0x0000	signed	CNTRLO 0xF556 0x0000 0x0AA9	CADC_S = [ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/2048) CADC_C = [ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/2048) Minimum value -2730 Mean value 0; no offset correction Maximum value +2729
15:0	CNTRLO_C	0x0000	signed		

ADC1	**ADC values channel 1**
ADC2	**ADC values channel 2**

31:16
ADC_S

15:0
ADC_C

Bit	Name	Reset value	Format	Value	Meaning
31:16	ADC_S	-	signed	0xE000 0x0000 0x1FFF	Minimum value -8192; corresponds to a differential voltage of approx. -495mV at the input of the instrumentation amplifier (@GAIN=00). Mean value 0; corresponds to a differential voltage of approx. 0mV at the input of the instrumentation amplifier. Maximum value +8191; corresponds to a differential voltage of approx. +495mV at the input of the instrumentation amplifier (@GAIN=00) .
15:0	ADC_C	-	signed		

CADC1	**Corrected ADC values channel 1**
CADC2	**Corrected ADC values channel 2**

In calibration mode (`CFG1/MODE = 0101`), the registers are refreshed by command `TRGCAL` or by an edge at the pin `TRG`. In the other operational modes, the registers always contain the actual corrected ADC-values.

31	30	29:16
VZ(CADC_S)	0	Abs(CADC_S)

15	14	13:0
VZ(CADC_C)	0	Abs(CADC_C)

Bit	Name	Reset value	Format	Value	Meaning
31	VZ(CADC_S)	-	Bit	0 1	Corrected ADC value sinusoidal ≥ 0 Corrected ADC value sinusoidal < 0
29:16	Abs(CADC_S)	-	unsigned	 0 0x3FFF	Corrected ADC value sinusoidal (absolute value) Minimum value Maximum value
15	VZ(CADC_C)	-	Bit	0 1	Corrected ADC value cosinusoidal ≥ 0 Corrected ADC value cosinusoidal < 0
13:0	Abs(CADC_C)	-	unsigned	 0 0x3FFF	Corrected ADC value cosinusoidal (absolute value) Minimum value Maximum value

Bit	Name	Reset value	Format	Value	Meaning
31:16	CADC_S	-	Sign + absolute value	CADC	Corrected ADC value sinusoidal `CADC_S = [ADC_S + CNTRLO_S] · (0.5 + CNTRLG_S/2048)`
15:0	CADC_C	-	Sign + absolute value	CADC	Corrected ADC value cosinusoidal `CADC_C = [ADC_C + CNTRLO_C] · (0.5 + CNTRLG_C/2048)`

IP11	**Interpolation register 1 – Angular value / angle difference – channel 1**
IP12	**Interpolation register 1 – Angular value / angle difference – channel 2**

31:16
DPHI

15:0
PHI

Bit	Name	Reset value	Format	Value	Meaning
31:16	DPHI	-	signed	DPHI	The value `DPHI` is the difference of the phase angle of sinusoidal and cosinusoidal signals between two samplings. The range of values is dependent on the set interpolation rate. This value represents the speed of the measuring system. $f_{Input} = DPHI/(96 \cdot IRATE) \cdot f_{OSZ}$
15:0	PHI	-	unsigned	0x0000 IRATE-1	The phase angle of sinusoidal and cosinusoidal signal is 0° The phase angle of sinusoidal and cosinusoidal signal is 360° - ε

IP21	***Interpolation register 2 – Angular value / controller value – channel 1***
IP22	***Interpolation register 2 – Angular value / controller value – channel 2***

In calibration mode (`CFG1/MODE = 0101`) this register contains a quadrant counter at the bits 31:16, which is refreshed by a trigger event or by the SPI command `TRGCAL`.

31:16
BQ

15:0
PHI

Bit	Name	Reset value	Format	Value	Meaning
31:16	BQ	-	unsigned	BQ	The value BQ contains the deviation of the gain and offset controller from the setpoint. If offset and gain are adjusted completely, the value of this register is 321.
15:0	PHI	-	unsigned	0x0000 IRATE-1	The phase angle of sinusoidal and cosinusoidal signal is 0° The phase angle of sinusoidal and cosinusoidal signal is 360° - ε

IP3	***Interpolation register 3 – Angular value 1 / Angular value 2***

31:16
PHI2

15:00:00
PHI1

Bit	Name	Reset value	Format	Value	Meaning
31:16	PHI2	-	unsigned	0x0000 IRATE-1	The phase angle of sinusoidal and cosinusoidal signal at channel 2 is 0° The phase angle of sinusoidal and cosinusoidal signal at channel 2 is 360° - ε
15:0	PHI1	-	unsigned	0x0000 IRATE-1	The phase angle of sinusoidal and cosinusoidal signal at channel 1 is 0° The phase angle of sinusoidal and cosinusoidal signal at channel 1 is 360° - ε

EEP	**EEPROM-Interface**

Read access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-				INIT	-	AUT	RSV	EEPVALID	EER	EWR	EEPBSY	EEPLOCK

15:0
EEPDAT

Bit	Name	Reset value	Format	Value	Meaning
24	INIT		Bit	1	This bit is reserved for test purposes.
22	AUT	0	Bit		This bit is reserved for test purposes.
21	RSV	0	Bit		This bit is reserved for test purposes.
20	EEPVALID	0/1	Bit	0	EEPROM valid identifier 0x134A at address 0x00 was not found
				1	EEPROM valid identifier 0x134A at address 0x00 was found. EEPROM content has been loaded into the registers during reset.
19	EER	0	Bit	0	No EEPROM delete access active.
				1	EEPROM delete access active.
18	EWR	0	Bit	0	No EEPROM write access active.
				1	EEPROM write access active.
17	EEPBSY	0	Bit	0	No EEPROM access active.
				1	EEPROM access active; No further command may be sent to the EEPROM.
16	EEPLOCK	0	Bit	0	The EPROM is free for use.
				1	EEPROM locked
15:0	EEPDAT	0x0000	binary		EEPROM-Data

Write access

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	EEPOPC			EEPADR							

15:0
EEPDAT

Bit	Name	Reset value	Format	Value	Meaning
26:24	EEPOPC	000	binary		EEP-OPCode; **Writing to this register triggers an EEPROM access.** The register must not be written if the `EEPBSY` is set. `EEPADR` and `EEPDAT` must be valid.
				000	NOP – No action
				001	WRITE – write 16 bit
				010	READ – read 16 bit
				100	ERASE – delete 16 bit
				other	Undefined behaviour. EEPROM content may be lost.
23:16	EEPADR	0x00	binary		EEPROM address. To program or read the EEPROM ,the address must be written to this register before activating the OPCode. The register must not be written if the bit `EEPBSY` is active.
15:0	EEPDAT	0x0000	binary		EEPROM-Data; To program the EEPROM, the data must be written to this register before activating the OP code. The register must not be written if the bit `EEPBSY` is set.

NONIUS *Nonius register*

31:16
KORR

15:0
GROB

Bit	Name	Reset value	Format	Value	Meaning
31:16	KORR	-	signed		Correction value calculated from the coefficients and the input signals. For test purpose only.
15:0	GROB	-	unsigned	0x0000 IRATE-1	Corrected nonius position (PHI1-PHI2) with a value range of 0 ... IRATE-1 For test purpose only.

10 Characteristic values

Table 42: Absolute maximum ratings

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Analog supply voltage			TBD [1]	V
VDD	Digital supply voltage			TBD [1]	V
TJ	Operating temperature	-40		125	°C
TS	Storage temperature	-55		150	°C
V(AIN)	Voltage at the analog inputs	-0.3		VDDA+0.3	V
V(DIN)	Voltage at the digital inputs	-0.3		VDDIO+0.3	V
ESD	ESD sensitivity (HBM)			2	kV

1) t < 250ms, T < 60°C

Table 43: Operating conditions

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VDDA	Analog supply voltage	3.15 (3.0) [1]	3.30	3.60	V
VDD	Digital supply voltage	3.00	3.30	3.60	V
I(VDDA)	Current consumption, analog		25		mA
I(VDD)	Current consumption, digital		25		mA
T	Operating temperature	-40		100 (125) [1]	°C

1) Controller ranges and interpolation accuracy are limited between 3.0V and 3.15V resp. between 100°C and 125°C.

Table 44: Characteristic values clock / reset

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{OSZ}	External Clock : frequency	4		26	MHz
TH/TL	External Clock : duty-cycle	40	50	60	%
t_{INIT}	Initialization time Time between `NRES` rising edge and Ready (`MISO,NERR`)		40	80	ms

Table 45: Characteristic values for interpolation

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{IP}	Input frequency (nonius calculation)	0		150	kHz
f_{IP}	Input frequency (interpolation)	0		90	kHz
IRATE	Interpolation rate (nonius calculation)	256		8192	Increments
IRATE_AB	Interpolation rate (ABZ)	32		8192	Increments
CTRL(A)	Amplitude control	60		120	%VINNOM[2]
CTRL(O)	Offset control	-15		15	%VINNOM[2]
VTH(INP)	Threshold voltage for vector monitoring		30		%VINNOM[2]
EABS	Absolute angle error[1]		TBD	TBD	Increments
EDIFF	Differential angle error[1]		TBD		Increments
tpp	Minimum edge distance A/B	$1/f_{OSZ}$		$128/f_{OSZ}$	ns
t(TRG)	Pulse width of the trigger signal	$3/f_{OSZ}$			ns
tp(Preset)	Pulse width PRESET signal	60			ms
td(CNT)	Delay time 'Analog input to nonius result'		$181/f_{OSZ} + 100$		ns
td(ABZ)	Delay time 'Analog input to A/B'		$208/f_{OSZ} + 100$		ns

1) Input voltage range 0.66 V_{pp} / matched phase deviation between sinusoidal and cosinusoidal signal
2) Nominal value of the differential voltage of SINP-SINN or COSP-COSN

Table 46: Digital characteristic values

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
VOH	Output voltage H	80			%VDDIO
VOL	Output voltage L			0.4	V
VIH	Input voltage H	70			%VDDIO
VIL	Input voltage L			30	%VDDIO
I(DIG1)	Output current digital			6	mA
I(DIG2)	Output current digital at `MISO` and `NERR`			12	mA
R(PU)	Internal Pull-Up resistors	90k		210	KΩ
R(PD)	Internal Pull-Down resistors	75k		250	KΩ

Table 47: Analog characteristic values

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
Z(AIN)	Input impedance		1GΩ||8pF		
Gain	Gain factor as per 10 @1kHz	97	100	103	%
fg	Cut-off-frequency analog low-pass-filter according to 11	90	100	110	%
fg_{MATCH}	Deviation of the cut-off-frequencies among the channels	-1	0	+1	%
V(AIN)	Voltage at the analog inputs	0.35		VDDA-1.0	V
CMIR	Common mode input voltage		1.1		V
CMRR	Common mode rejection ratio (@ f < 1kHz, `GAIN` maximum)	65			dB
V(V0)	Voltage at pin `V0` / DC-voltage at `SMON/CMON`	1.08	1.1	1.12	V
VMON	AC-voltage at `SMON/CMON` @ nominal amplitude		1.27		V_{pp}
I(V0)	Output current at `V0`			1	mA
CL(V0)	Capacitive load at Pin `V0`			300	pF
VTH(REF)	Switching threshold reference-point-comparator 2)	-1		1	mV
VH(REF)	Hysteresis reference-point-comparator 2)		15		%VINNOM1)
I(OUTX)	Output current at pin `SMON1/CMON1/SMON2/CMON2`			0.5	mA
CL(OUTX)	Capacitive load at pin `SMON1/CMON1/SMON2/CMON2`			50	pF
φK1	Phase correction in range 1	± 4.5	± 5	± 5.5	°
φK2	Phase correction in range 2	± 9	± 10	± 11	°

1) Nominal value of the difference voltage of `SINP-SINN` or `COSP-COSN`

2) Voltage difference `REFP-REFN`

Table 48: Characteristic values EEPROM

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
$t_{READEEP}$	EEPROM read duration	20		85	us
$t_{PROGEEP}$	Programming time / delete time	4	9.5	11	ms
$t_{RETENTIONEEP}$	Data retention @ T < 85°	10			Years
$N_{ProgEEP}$	Endurance @ T = 25° @ T = 125°	10^4 10^3			Write cycles

Table 49: Characteristic values SSI interface

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{MA}	Clock frequency @ $f_{OSZ} \geq 4MHz$ @ $f_{OSZ} \geq 8MHz$ @ $f_{OSZ} \geq 10MHz$ @ $f_{OSZ} \geq 20MHz$			2 3 4 5	MHz
t_D(MISO)	Delay time `MA` rising until `SLO`			25	ns
$t_{TIMEOUT}$	Timeout → `CFGBISS`	3/f_{OSZ}	10	4095 / f_{OSZ}	us

Table 50: Characteristic values BiSS interface

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
f_{MA}	Clock frequency			10	MHz
t_D(MISOBISS)	Delay time `MA` rising until `SLO`			20	ns
t_{BUSY_S}	Start bit delay SCD		0		ns
t_{BUSY_R}	Start bit delay Register data		0		ns
t_{BUSY_E}	Start bit delay EEPROM data		$t_{READEEP}$		ns
$t_{TIMEOUT}$	Timeout → `CFGBISS`	$2/f_{OSZ}$	25	$2^{31}/f_{OSZ}$	us

Table 51: Characteristic values SPI interface

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
t_{HIGH}(SCK)	SPI-Clock, H time	20			ns
t_{LOW}(SCK)	SPI-Clock, L time	20			ns
t_S(SEN)	Setup time `SEN` falling before `SCK` rising	15			ns
t_H(SEN)	Hold time `SEN` rising after `SCK` falling	15			ns
t_s(MOSI)	Setup time `MOSI` before `SCK` rising	5			ns
t_H(MOSI)	Hold time `MOSI` after `SCK` rising	5			ns
t_D(MISO)	Delay time `SCK` falling until `MISO` @CL = 12 pF			20	ns
t_{ENA}(MISO) [1]	Delay time `SEN` falling until `MISO` active			25	ns
t_D(nWAIT)	Delay time `SEN` rising until `nWAIT` active		60	70	ns
t(nWAIT-L)	Waiting time after `SEN` rising	$2/f_{OSZ}$		$4/f_{OSZ}$ + 25	ns
	Waiting time after `SEN` rising (synchronous read)	$2/f_{OSZ}$		$36/f_{OSZ}$ + 25	ns
t(SEN-Wait)	Time between wait state and next access	0			ns

[1] for non-read commands, the pin `MISO` may remain in the tristate state (inactive).

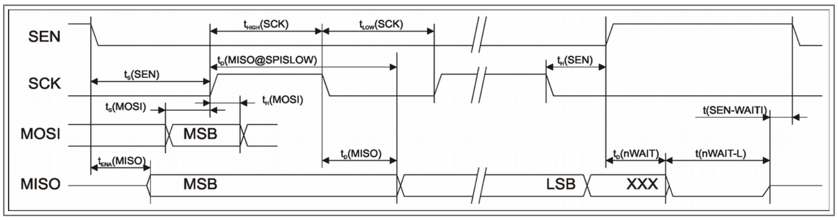


Figure 31: Timing SPI

Table 52: Characteristic values Simple-SPI-Master

Symbol	Characteristic value	Min.	Typ.	Max.	Unit
t_{HIGH}(SCK)	SPI clock, H time		$1/f_{OSZ}$		ns
t_{LOW}(SCK)	SPI clock, L time		$1/f_{OSZ}$		ns
t_s(MISO)	Setup time `MISO` before `SCK` rising	5			ns
t_H(MISO)	Hold time `MISO` after `SCK` rising	5			ns
t_D(MOSI)	Delay time `SCK` **falling** until `MOSI` @CL = 12 pF			20	ns
t_{TXENA}	Pulse width `TXENA` (High)			TBD/f_{OSZ}	ns

11 Application notes

11.1 Application circuit

As the GC-NIP includes two fast A/D converters, the same design rules applicable to A/D converters must be applied. All block capacitors are to be connected closely to the pad. Please note that the quality of the sensor power supply also influences the measuring accuracy of standard sensors. If necessary, additional LC filters to the sensor power supply and to AVDD must be included.

The supply- and reference-voltage pins are to be connected as seen in 53; the connection of unused inputs is shown in 54.

Table 53: IC connection, voltages

Pin	Connection
VSSA	Ground analog
VSS, VSSIO, Exposed Pad	Ground digital
VDDA	Supply voltage analog 3.3V Block capacitor 100nF against VSSA
VDD, VDDIO	Supply voltage digital 3.3V Block capacitor 100nF against VSS/VSSIO
R1N,R1M,R1P,R2N,R2M,R2P	a block capacitor each 2.2µF against VSSA and a block capacitor each 10nF against VSSA
V01,V02	A block capacitor 100nF against VSSA open input possible if CFG2/DISV0 = 1

Table 54: IC connection of unused in-/outputs

Pin	Connection, if unused
NRES	Pull-Up 10k against VDDIO
SINN, COSN, REFN	V0
REFP	AVDD or AVSS
CFGAF, CFGGAIN, CFGDIR	VSSIO
PRESET, TXENA/TRG	VDDIO
MISO/SLO	Pull-Up 1k against VDDIO
MOSI/SLI	VSSIO
SCK/MA	VSSIO
SEN	VDDIO
NERR	Pull-Up 10k against VDDIO
TM	VSS

General notes:

- All block capacitors have to be connected closely to the pad.
- Separate ground areas for `VSSA` resp. for `VSS` and `VSSIO` must be used.
- The ground areas for `VSSA` and `VSS/VSSIO` must be connected at one point of the PCB.
- The pins `NRES`, `NERR` require a pull-up resistor of 10 kΩ each.
- The pin `MISO/SLO` requires a pull-up resistor of 1 kΩ.
- For using the SPI with high data rates, series resistors of 22...33 Ω each at `MOSI`, `MISO`, `SCK` and `SEN` are useful.
- The digital outputs `A`, `B` and `Z` are designed for a maximum load of 6 mA. An external driver-IC is necessary to realize a differential RS422-interface. The outputs can be configured for tristate behaviour in case of error. Depending on the application, pull-up resistors are required.
- For the use of additional termination resistors between `SINP` and `SINN` respectively between `COSP` and `COSN` please refer to the application notes of the sensor manufacturer.
- Single-ended sensors are typically connected to the inputs `SINP` and `COSP`. The DC reference levels of the GC-NIP and of the sensor must concordant in this case.
- The signals `V01` and `V02` can be used as reference level. The current rating at this pins totals 1 mA. Short and low-capacity wires should be used. A buffer operational amplifier may be included, if necessary.
- For reliable operation of the IC, it is imperative to connect defined levels to the IC inputs. Internal pull-up resistors only prevent unpredictable behaviour of the IC with floating inputs.

The design of the analog input circuit depends on the type of the sensor that is connected. The following figures show an example of one channel connected to different types of sensors:

Sensor with differential output signals

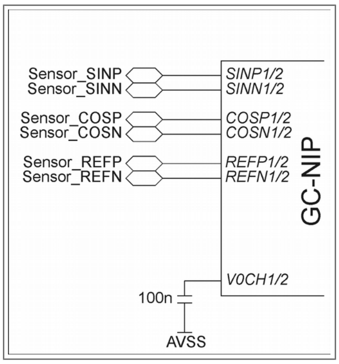


Figure 32: Sensor with differential output signals

The amplitude of the sensor and the gain factor of the GC-NIP are adapted by the configuration bits GAIN(1:0)
Reference level V0 is generated internally.

Sensor with a nominal amplitude of 1V_{pp} or 2V_{pp}

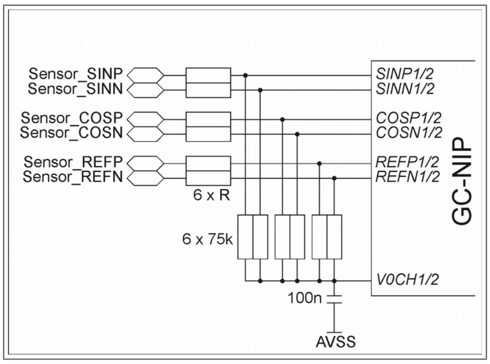


Figure 33: Sensor with a nominal amplitude of 1Vpp or 2Vpp

The nominal amplitude of the GC-NIP is configured to the value 660 mVpp using the bits GAIN(1:0).
Reference level V0 is generated internally.
External resistors between the input signals and pin V0 are used as voltage divider for the sensor signals. The value for the resistor is calculated as follows: R = (V_{Sensor} / 660mV - 1) · 75 kΩ
The amplitude of the sensor signals and the reference level will be divided using the ratio R/75kΩ.
Alternatively, for sensors with 5V supply, the level-shifter-IC *GC-LS* can be used.

Sensor with single-ended output signals (1)

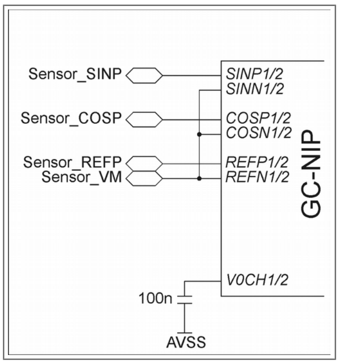


Figure 34: Sensor with single-ended output signals (1)

The amplitude of the sensor and the gain factor of the GC-NIP are adapted by the configuration bits GAIN(1:0)
Reference level V0 Is generated by sensor.

Sensor with single-ended output signals (2)

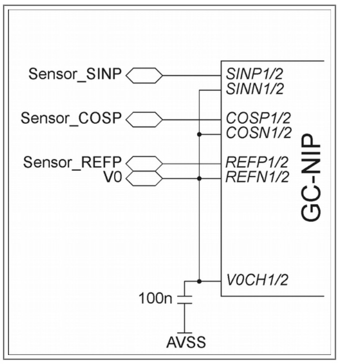


Figure 35: Sensor with single-ended output signals (2)

The amplitude of the sensor and the gain factor of the GC-NIP are adapted by the configuration bits GAIN(1:0)
Reference level V0 is generated internally an is provided to the sensor.

Sensor containing antiparallel photodiodes Adjustment of amplitude equality possible

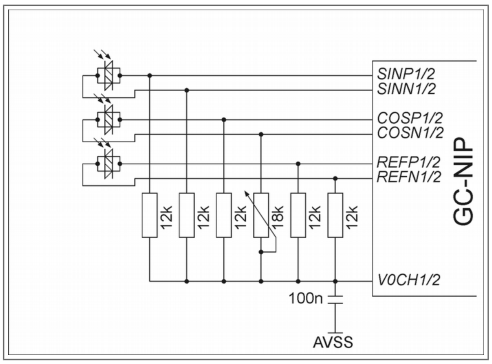


Figure 36: Sensor containing antiparallel photodiodes

The nominal amplitude of the GC-NIP has to be set to 250mVpp by configuration bits GAIN(1:0).
Reference level V0 is generated internally.
The amplitude equality is adjusted by changing the amplitude of the cosine signal. The pins SMON and CMON are used for the measurement.
The value of the resistors has to be adjusted to the given sensor:
$R_{FIX} = 250\text{ mV} / (2 \cdot I_{SENSOR})$ and $P_{AMPL} \approx 1.5 \cdot R_{FIX}$
Example: $I_{SENSOR} = 11\ \mu A_{pp}$

Array of photo diodes with common cathode or anode Adjustment of amplitude equality and offset possible

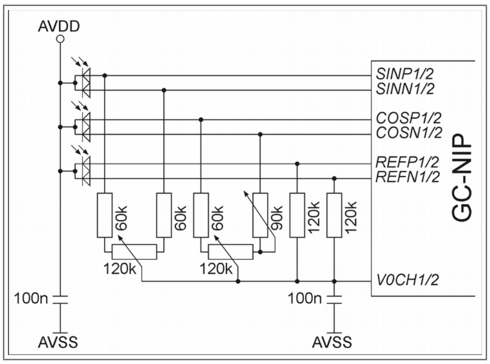


Figure 37: Array of photo diodes with common cathode or anode

The nominal amplitude of the GC-NIP has to be set to 160mVpp by configuration bits GAIN(1:0).
Reference level V0 is generated internally.
The amplitude equality is adjusted by changing the amplitude of the cosine signal. Thereafter the offset for both signals can be adjusted. The pins SMON and CMON are used for the measurement.
The values of the resistor has to be adjusted to the given sensor:
$R = 160\text{mV} / (2 \cdot I_{SENSOR})$.
This resistor is partly designed as a potentiometer for the adjustment of the offset
$P_{OFFS} \approx R$; $R_{FIX} \approx ½ R$; $P_{AMPL} \approx 1.5 \cdot R_{FIX}$
Example: $I_{SENSOR} = 0.5\ \mu A_{pp}$

Sensor for current signals 11 μA_{pp}

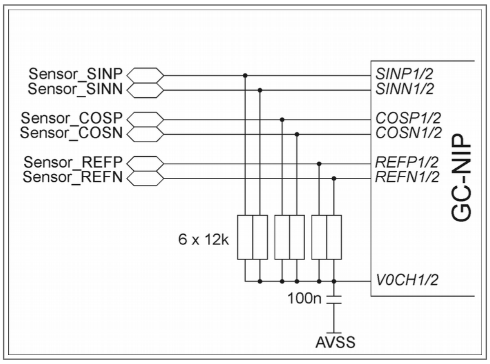


Figure 38: Sensor for current signals 11 µApp

The nominal amplitude of the GC-NIP is set to 250mVpp by configuration bits GAIN(1:0).
Reference level V0 is generated internally.
The value of the resistor R is dimensioned as follows:
$R = 250\text{mV} / (2 \cdot I_{SENSOR})$
Example: $I_{SENSOR} = 11\ \mu A_{pp}$

The following figures show examples for the connection of the various interfaces:

ABZ Output / Configuration via pin

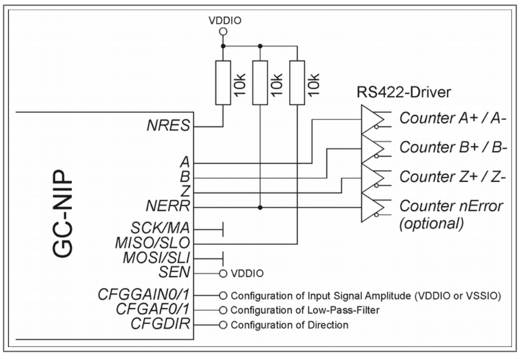


Figure 39: ABZ Output / Configuration via pin

The nominal amplitude and the low-pass filter frequency are set via configuration pins. All other configurations are set as in Table 8.
Connection of the second ABZ output is identical.

ABZ Output / Configuration via EEPROM

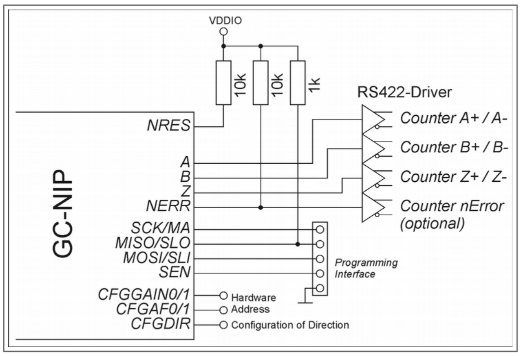


Figure 40: ABZ Output / Configuration via EEPROM

The configuration of the IC is read from the integrated EEPROM.
The SPI interface is used as programming interface to the EEPROM
Short wires should be used at the pins `MOSI`, `SEN` and `SCK`.
Otherwise, pull-up resistors (10 kΩ) are recommended.
Connection of the second ABZ output is identical.

SPI interface LVDS

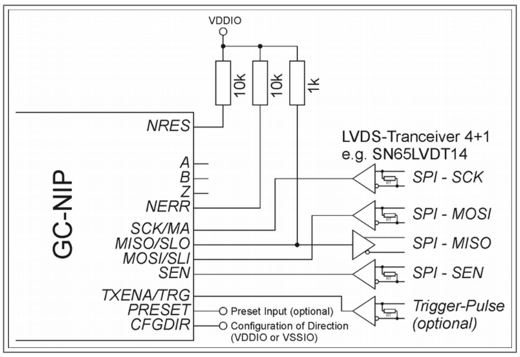


Figure 41: SPI interface LVDS

The IC is configured from the internal EEPROM or via the SPI interface.
The LVDS driver IC enables long cable length at high clock frequencies.
The trigger pulse is provided as differential signal (optional).

SPI interface to PC via USB

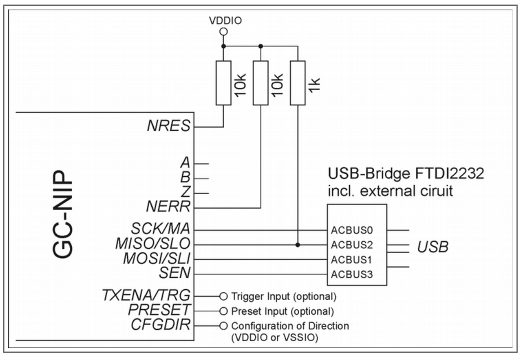


Figure 42: SPI interface USB

The IC is configured from the internal EEPROM of via the SPI interface.
SPI communication is realized using a bridge-IC with USB interface to the PC.

BiSS interface

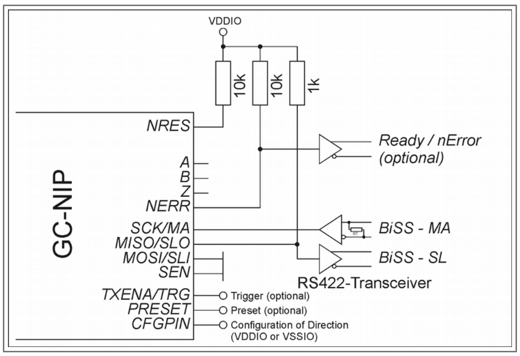


Figure 43: BiSS interface

The configuration of the IC is read from the integrated EEPROM.
BiSS is used as point-to-point connection.
An optional signal indicates the ready/error status if the GC-NIP.

SSI interface

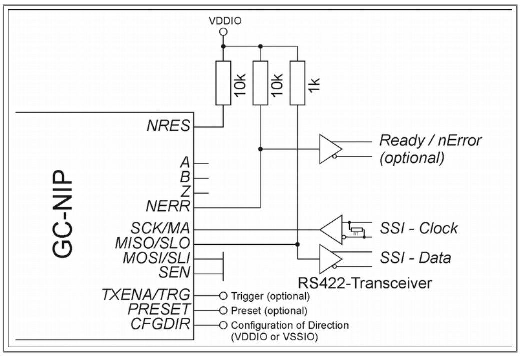


Figure 44: SSI interface

The configuration of the IC is read from the integrated EEPROM.
An optional signal indicates the ready/error status if the GC-NIP.

SPI interface to microcontroller

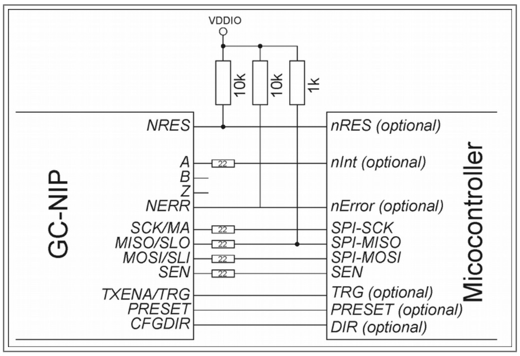


Figure 45: SPI interface to microcontroller

The IC is configured from the internal EEPROM or via the SPI interface.
The microcontroller firmware implements the SPI master for communication to the GC-NIP.
An optional signal is used as trigger, another as interrupt to the microcontroller.
Optionally, the controller is able to reset the GC-NIP.

Simple SPI to additional microcontroller

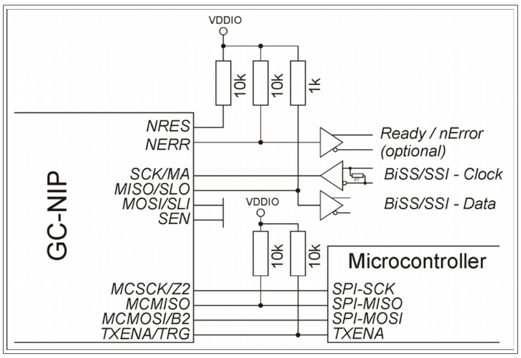


Figure 46: SSI-/BiSS interface and Simple SPI master

The configuration of the IC is read from the integrated EEPROM.
The measurement values are output via the BiSS- or SSI-interface.
An external microcontroller enables read and modify of the measurement value. The communication is controlled by the pin `TXENA/TRG`.

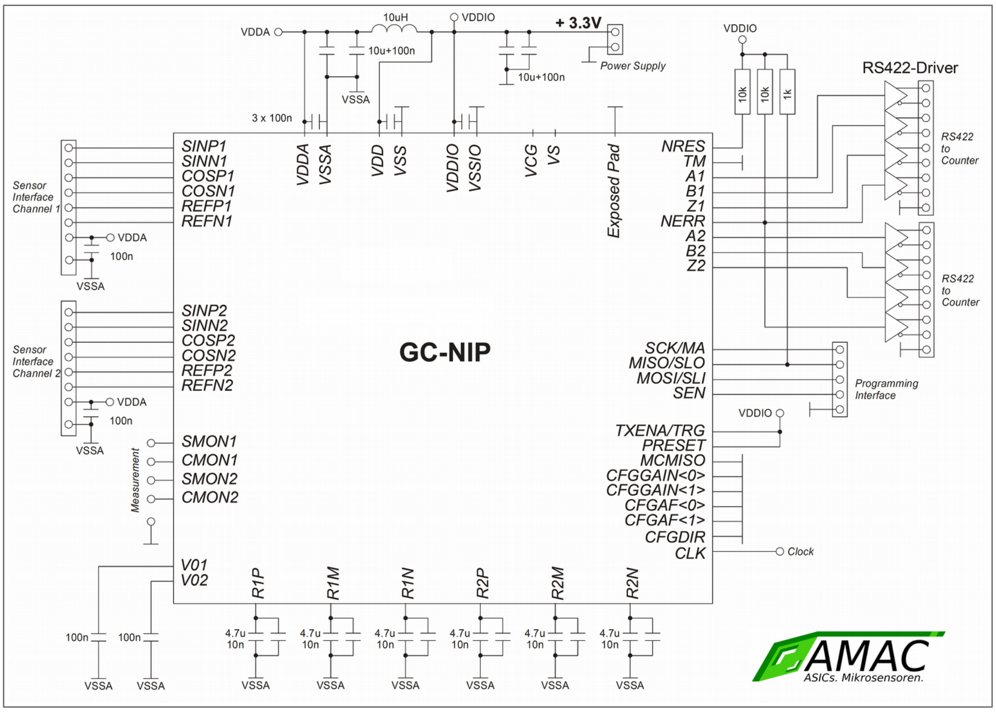


Figure 47: Minimum application circuit (principle)

- The configuration of the IC is read from the integrated EEPROM.
- The SPI interface is used for programming of the EEPROM and for calibration of the nonius scale.
- Short wires should be used at the pins `MOSI`, `SEN` and `SCK`. Otherwise, pull-up resistors (10 kΩ) are recommended.

For further information for connection of the IC and usage of the interfaces please request the detailed circuit of the evaluation board „GP-NIP“ and the recommended PCB-layout via E-Mail to support@amac-chemnitz.de.

11.2 Fast equidistant measurements via SPI

Fast and/or equidistant measurements can be realized via the SPI interface:

Table 55: Equidistant measurements

Time base	Pin `TRG`	SPI interface	Remark
From the SPI-interface	For asynchronous trigger events	SYNC mode	Enabling `SEN` with a period of $N \cdot 96/f_{OSZ}$ allows equidistant measurement without jitter. Exact synchronization of several ICs is possible.
External	Time base	ASYNC mode	Jitter: $96/f_{OSZ}$. Reading of the measures values via SPI must be completed within the measuring interval. Exact synchronization of several ICs is possible.

11.3 Program sequence examples

A measurement example using the trigger and measurement value register `MVAL` is shown in the following figure. The determination of the trigger values and the sensor monitoring is done using the register `STAT`:

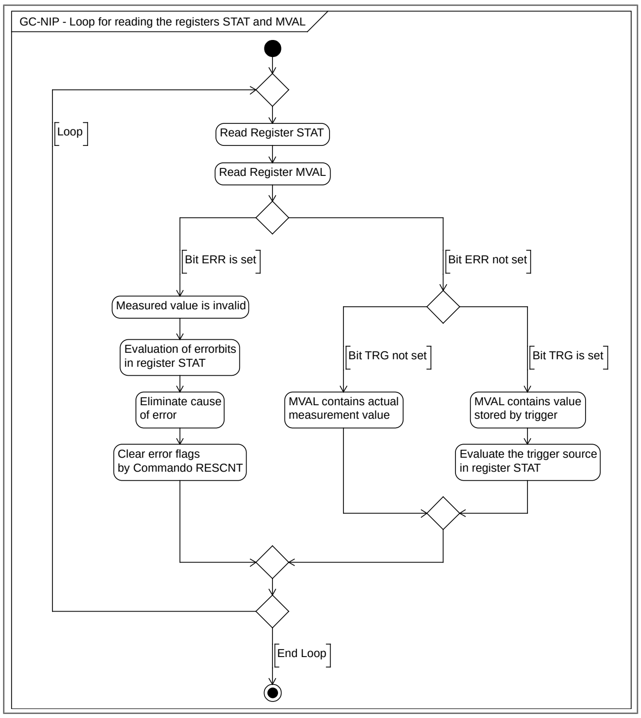


Figure 48: Program sequence for reading MVAL and STAT

For adjustment of the reference position and for evaluation of distance coded reference marks, the sequence can be extended (see sections 7.6.3 and 11.5 for further information):

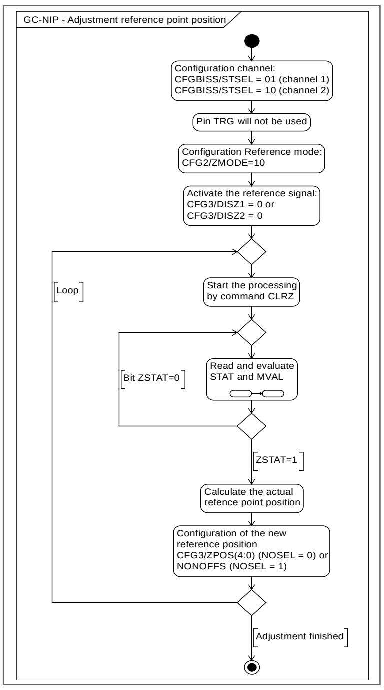


Figure 49: Extended programming sequence for ZMODE 10

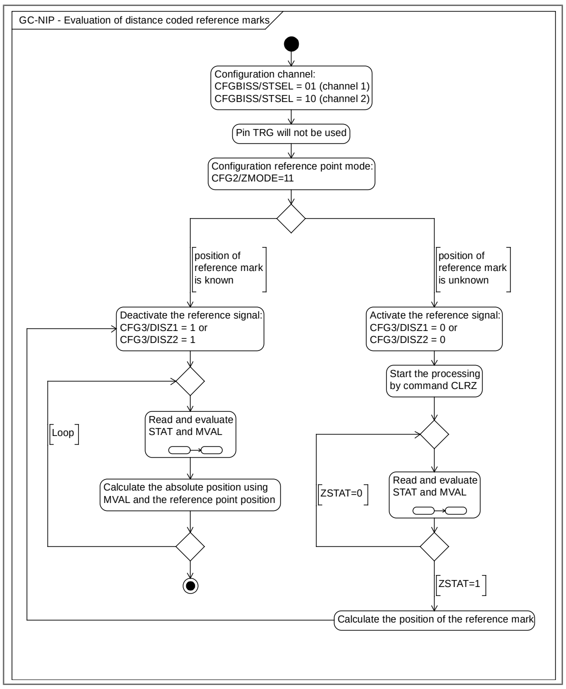


Figure 50: Extended programming sequence for ZMODE 11

see section 7.6.3 and 11.5

11.4 EEPROM

Reading from and writing to the EEPROM is handled by an internal interface, which can be accessed using the register `EEP` :

Before any write access, the bit EEPBSY must contain the value '0'
Writing an OP-code to the register EEPOPC (Byte 3) trigger a EEPROM access. EEPADR and EEPDAT must be valid.
Invalid OP-codes shall not be used.

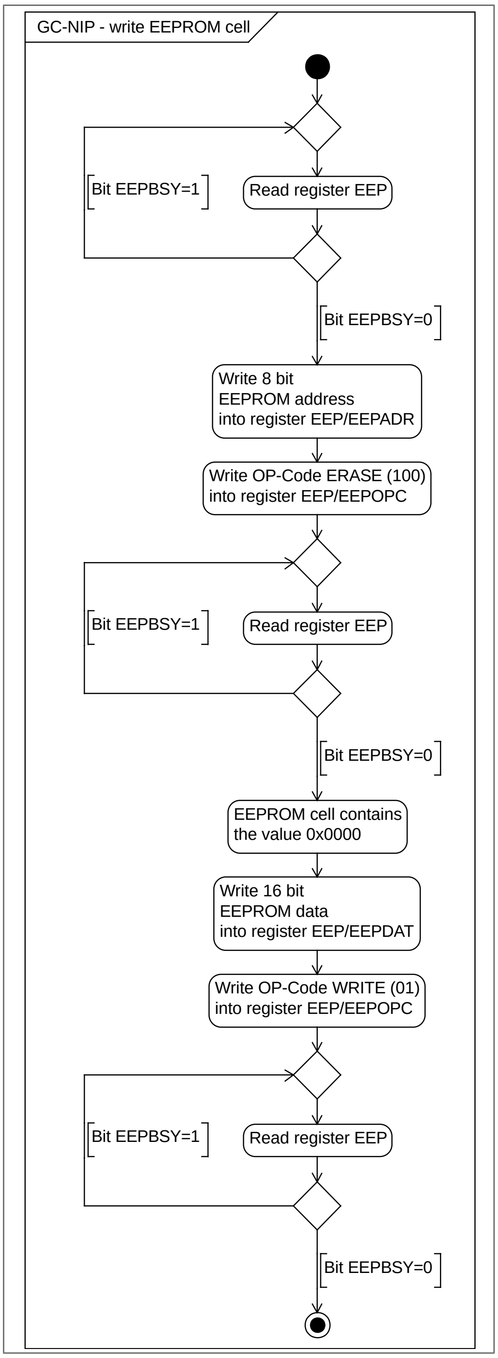


Figure 51: Programming sequence write/read EEPROM

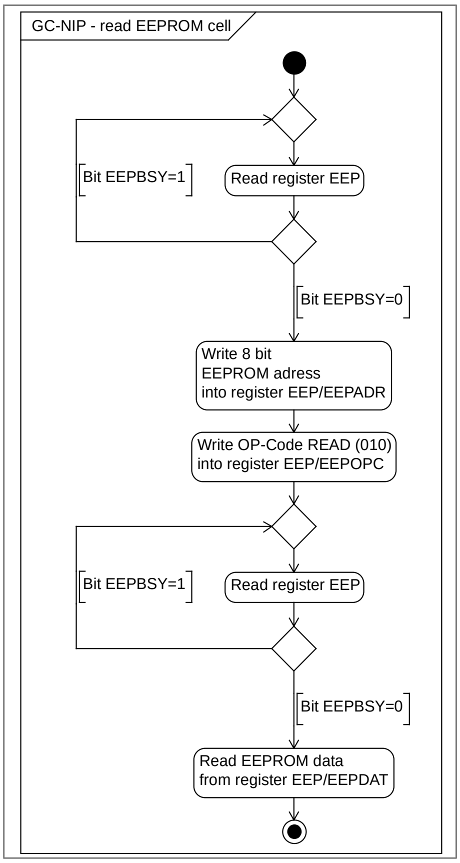


Figure 52: Programming sequence write/read EEPROM

11.5 Evaluation of distance-coded reference marks

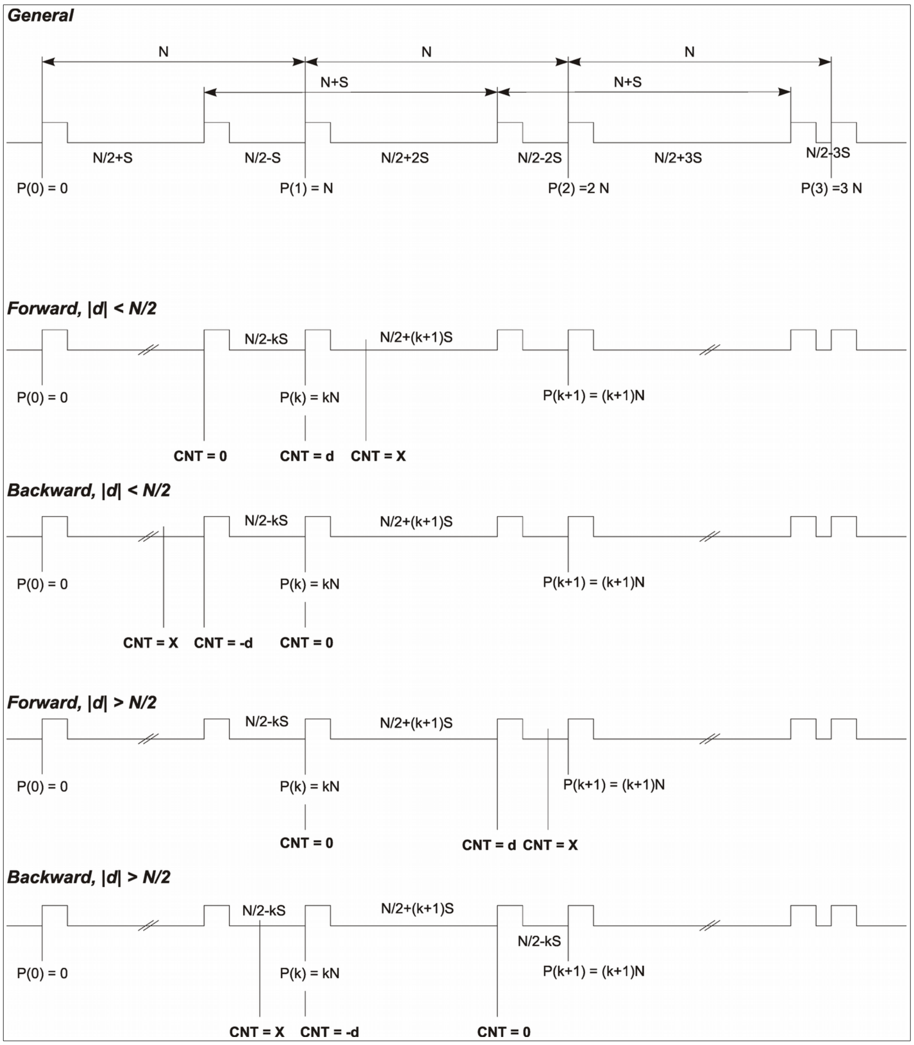


Figure 53: Evaluation of distance-coded reference marks

Table 56: Evaluation of distance-coded reference marks

0<d< ½·N **Figure 53-1**	**-½·N<d<0** **Figure 53-2**	**½·N<d** **Figure 53-3**	**d<-½·N** **Figure 53-4**
D = d/IRATE·M	D = d/IRATE·M	D = d/IRATE·M	D = d/IRATE·M
D = (N/2-k·S)	D = -(N/2-k·S)	D = N/2+(k+1)·S	D = -N/2-(k+1)·S
P = N/S·(N/2-D)	P = N/S·(N/2+D)	P = N/S·(D-N/2)-N	P = -N/S·(D+N/2)-N
PX = P-D+X/IRATE·M	PX = P+X/IRATE·M	PX = P+X/IRATE·M	PX = P-D+X/IRATE·M

With:

`M:` Scale graduation (mm)
`N:` Segment length of the reference mark on the scale (mm)
`S:` Reference point step width on the scale (mm)
`k:` Reference mark number on the scale
`P(k):` Absolute position of the reference mark k (mm)
`d:` Triggered reference mark distance (increments)
`D:` Triggered reference mark distance (mm)
`X:` Counter value (increments)
`PX:` Absolute position of the sensor (mm)

11.6 Configuring t_{pp} and f_{osz}

The GC-NIP is configured according to the requirements of the sensor and of the subsequent electronics. Also see sections 7.3 and 7.4

Table 57: Configuration tpp and speed monitoring

<table>
<tr><th colspan="4">ABZ output used?</th></tr>
<tr><th colspan="2">no</th><th colspan="2">yes</th></tr>
<tr><td colspan="2">CFG1/MABZ=0
CFG1/TPP(2:0)any value</td><td colspan="2">CFG1/MABZ=1
CFG1/MFAST=1
Condition: $t_{pp\ (counter\ at\ ABZ)} < t_{pp\ (GC\text{-}NIP)}$</td></tr>
<tr><th colspan="2">Interpolation counter used ?</th><th colspan="2">Oscillator frequency specified?</th></tr>
<tr><th>no</th><th>yes</th><th>no</th><th>yes</th></tr>
<tr><td rowspan="2">CFG1/MFAST=0
$f_{MAX} \geq 150kHz$</td><td rowspan="2">CFG1/MFAST=1
$f_{MAX} = f_{OSZ} / 280$</td><td>`CFG1/TPP(2:0)` any value
typical: `CFG1/TPP(2:0)='001'`
$N = 2^{CFG1/TPP(2:0)}$
$4\ MHz \leq f_{OSZ} < N/t_{pp\ (counter\ at\ ABZ)} \leq 26\ MHz$</td><td>$N = 2^{CFG1\text{-}TPP(2:0)} > t_{pp\ (counter\ at\ ABZ)} \cdot f_{OSZ}$</td></tr>
<tr><td colspan="2">t_{pp} (GC-NIP) = N / fOSZ
$f_{MAX} < 0.9 \cdot f_{OSZ} \cdot IRDIV / (N \cdot IRATE)$ **and** $f_{MAX} < f_{OSZ} / 280$</td></tr>
</table>

Example a)

The minimum edge distance of the electronics connected to `A`, `B` and `Z` is 250 ns.
The interpolation rate is 4000, IRDIV is configured to '10' (4) (interpolation rate ABZ = 1000).
The maximum input frequency is 2 kHz.
The oscillator frequency can be selected freely within the range 4 MHz ... 26 MHz.

`CFG1/MFAST = 1`
`CFG1/MABZ = 1`
`CFG1-TPP(2:0)='001'` → **N = 2**
$f_{OSZ} < 2/250ns$, $2kHz > 0.9 \cdot f_{OSZ} \cdot 4 / (2 \cdot 4000)$
→ **4.44 MHz <** f_{OSZ} **< 8 MHz**
	`CFG1/MFAST = 1`
	`CFG1/MABZ = 1`
	`CFG1-TPP(2:0)='010'` → **N = 4**
	$f_{OSZ} < 4/250ns$, $2kHz > 0.9 \cdot f_{OSZ} \cdot 4 / (4 \cdot 200)$
	→ **8.88 MHz <** f_{OSZ} **< 16 MHz**

Example b)

The minimum edge distance of the electronics connected to `A`, `B` and `Z` is 150 ns.
The interpolation rate is 2000, IRDIV is configured to '11' (8) (interpolation rate ABZ = 250).
The oscillator frequency is 26 MHz.
The maximum input frequency is determined on the basis of the specified parameters.

`CFG1/MFAST = 1`
`CFG1/MABZ = 1`
$N = 2^{CFG1\text{-}TPP(2:0)} > 150\ ns \cdot 26\ MHz \rightarrow N > 3.9$
`CFG1-TPP(2:0)='010'` → **N = 4**
$f_{MAX} = 0.9 \cdot 26\ MHz \cdot 8 / (4 \cdot 2000)$
$\mathbf{f_{MAX} = 23.4\ kHz}$

11.7 Configuration of the interface SPI/BiSS/SSI

The interface of the GC-NIP is configured according to the requirements of the interface master and the data format of the position value. See sections 8.1, 8.2, 8.3 and 7.8.

Example a) SPI-Mode
Maximum data rate for reading the counter value and the status information.

Configuration	Value	Details
CFG2/ASYNC	1	Maximum data rate
CFG2/SYNC	any value	Any value for `SYNC(6:0)` for reading `CNT1` and `CNT2`
CFGBISS/STSEL	any value	Register `POSIT` is not used
CFGBISS/STBIT	any value	Register `POSIT` is not used
CFGBISS/GRAY	any value	Register `POSIT` is not used
CFGBISS/READ32	any value	BiSS-Interface inactive
CFGBISS/BISSTO	any value	BiSS-Interface inactive
CFGBISS/RING	any value	SSI-Interface inactive
CFGBISS/SSITO	any value	SSI-Interface inactive
CFGBISS/SSI20	any value	SSI-Interface inactive

Example b) SPI-Mode
Reading of all data registers using a software timer.

Configuration	Value	Details
CFG2/ASYNC	0	(equidistant) measurement triggered by software timer
CFG2/SYNC	64dez	Reading of some registers requires this value
CFGBISS/STSEL	00bin	Register `POSIT` contains the absolute position (nonius), Register `CNT1` and `CNT2` contains the incremental value of the interpolation counters
CFGBISS/STBIT	30dez	The maximum number of bits is used
CFGBISS/GRAY	0	Usually, binary data is transferred via the SPI interface
CFGBISS/READ32	any value	BiSS-Interface inactive
CFGBISS/BISSTO	any value	BiSS-Interface inactive
CFGBISS/RING	any value	SSI-Interface inactive
CFGBISS/SSITO	any value	SSI-Interface inactive
CFGBISS/SSI20	any value	SSI-Interface inactive

Example c) BiSS-C-Mode
The measurement value is binary coded
The clock frequency of the GC-NIP is 26MHz.
Register access via the BiSS interface is only used for reading and writing configuration registers.

Configuration	Value	Details
CFG2/ASYNC	any value	No register access to data (measurement) registers.
CFG2/SYNC	any value	No register access to data (measurement) registers.
CFGBISS/STSEL	00bin	The BiSS-SCD (and register `POSIT`) provides the nonius result.
CFGBISS/STBIT	30dez	30 Bit single-turn data, two leading zero bits are added to get the total length of 32 bit.
CFGBISS/GRAY	0	Binary code
CFGBISS/READ32	0	No register access to data (measurement) registers.
CFGBISS/BISSTO	9	BiSS-Timeout = 512/26 MHz = 19.7 µs
CFGBISS/RING	any value	SSI-Interface inactive
CFGBISS/SSITO	any value	SSI-Interface inactive
CFGBISS/SSI20	any value	SSI-Interface inactive

Example d) SSI-Mode 20 bit
The measurement value is transferred in gray-code.
The clock frequency of the GC-NIP is 8MHz.
The SSI-Master operates in ring-mode with a timeout of 18 µs.

Configuration	Value	Details
CFG2/ASYNC	any value	any value for SSI
CFG2/SYNC	any value	any value for SSI
CFGBISS/STSEL	00bin	The SSI data (and register `POSIT`) provides the nonius result.
CFGBISS/STBIT	30dez	The maximum number of bits is used
CFGBISS/GRAY	1	Gray code
CFGBISS/READ32	any value	BiSS-Interface inactive
CFGBISS/BISSTO	any value	BiSS-Interface inactive
CFGBISS/RING	1	Ring operation possible
CFGBISS/SSITO	141dez	SSI timeout = 144 / 8 MHz = 18µs
CFGBISS/SSI20	1	SSI interface is working with 20 bit

11.8 BiSS configuration file idbiss4743.xml

To enable auto detection of the GC-NIP on a BiSS master device, the configuration file *idbiss4743.xml* can be used. For the detection of the data format of the single-cycle-data (SCD), it is recommended to program the BiSS vendor identifier according to the data format selected in `CFGBISS/STSEL` (see the following table and section 7.8).

CFGBISS/STSEL	Recommended vendor identifier	SCD (Pos 0)	SCD (Pos 1)	SCD (Pos 2)	SCD (Pos 3)
00bin	0x32 0x03 0x00 0x00	10 bit unused	22 bit Nonius	1 bit error	1 bit warning
01bin	0x32 0x03 0x01 0x00	2 bit unused	30 bit counter 1	1 bit error	1 bit warning
10bin	0x32 0x03 0x02 0x00	2 bit unused	30 bit counter 2	1 bit error	1 bit warning
11bin	0x32 0x03 0x03 0x00	16 bit counter 1	16 bit counter 2	1 bit error	1 bit warning

Notes